

Fig. 1
Prior Art

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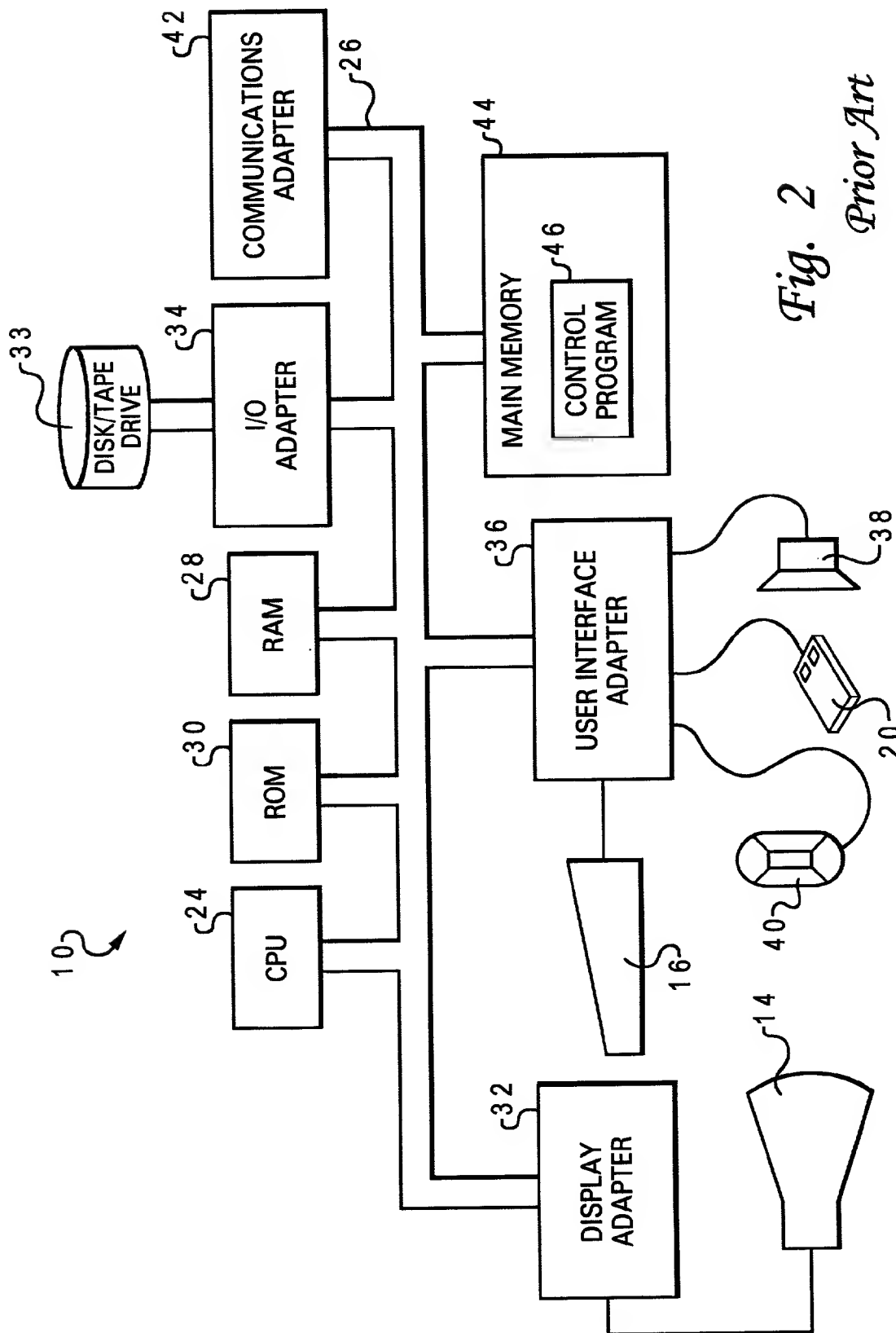


Fig. 2
 Prior Art

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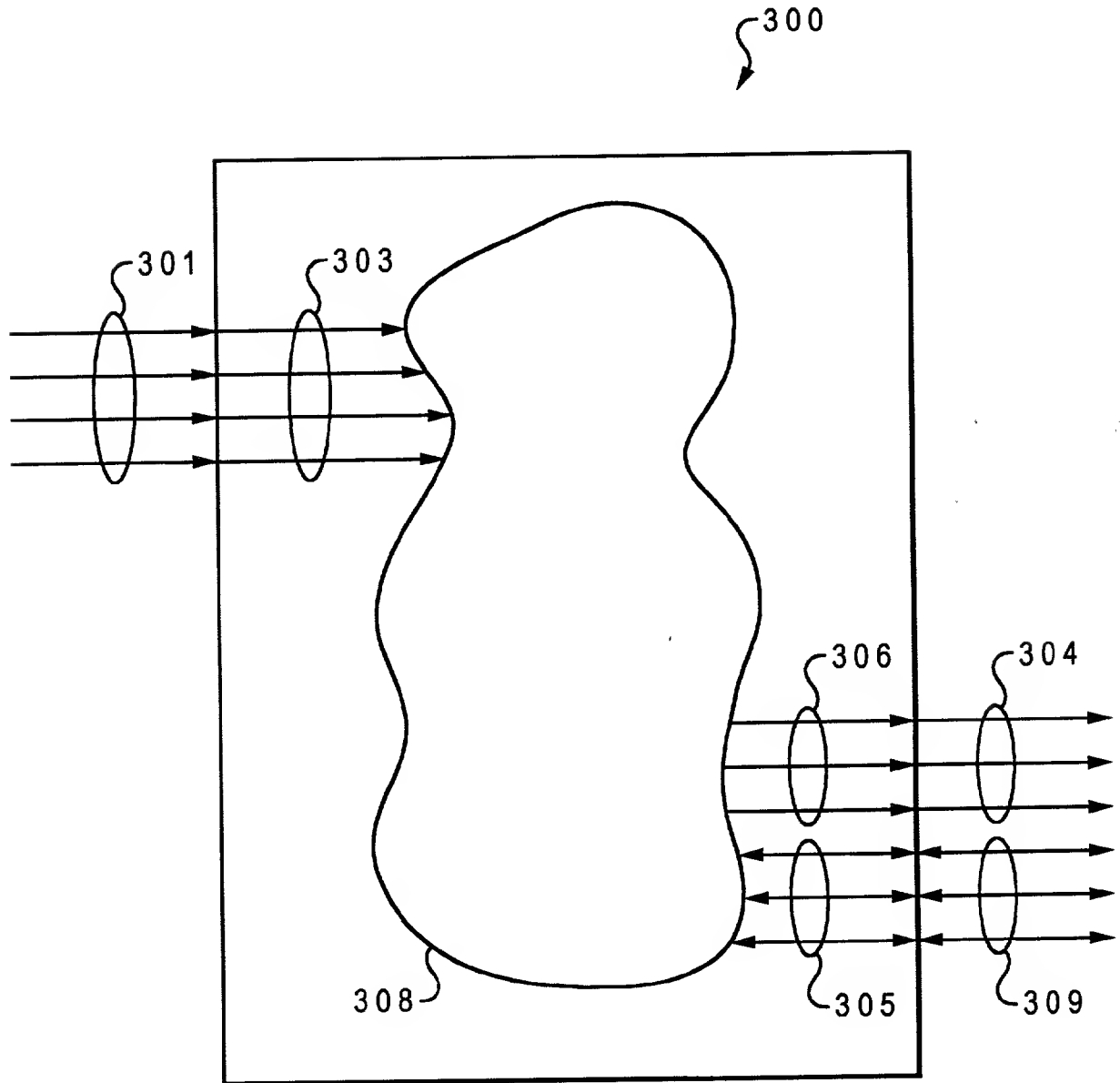


Fig. 3A

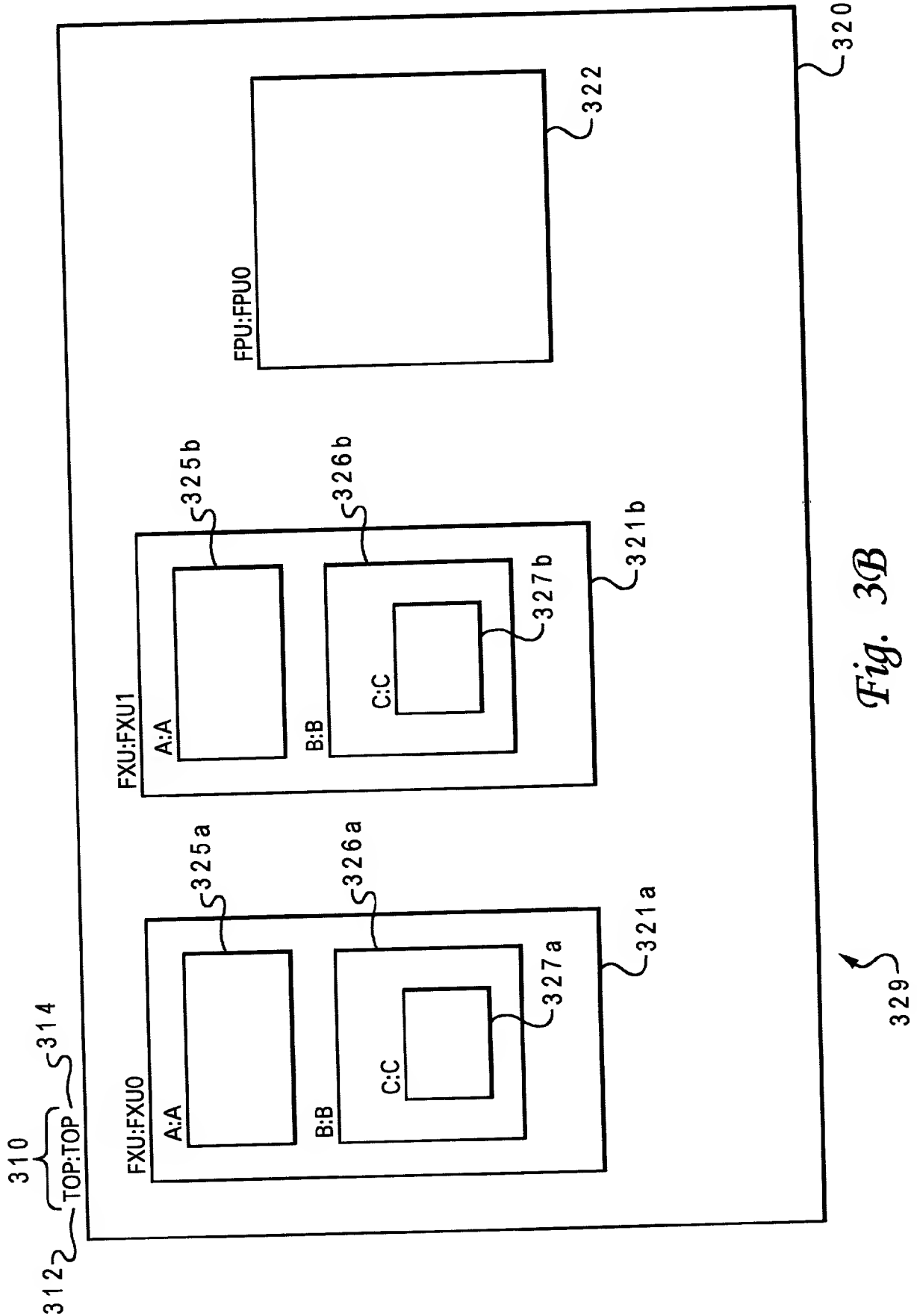


Fig. 3B

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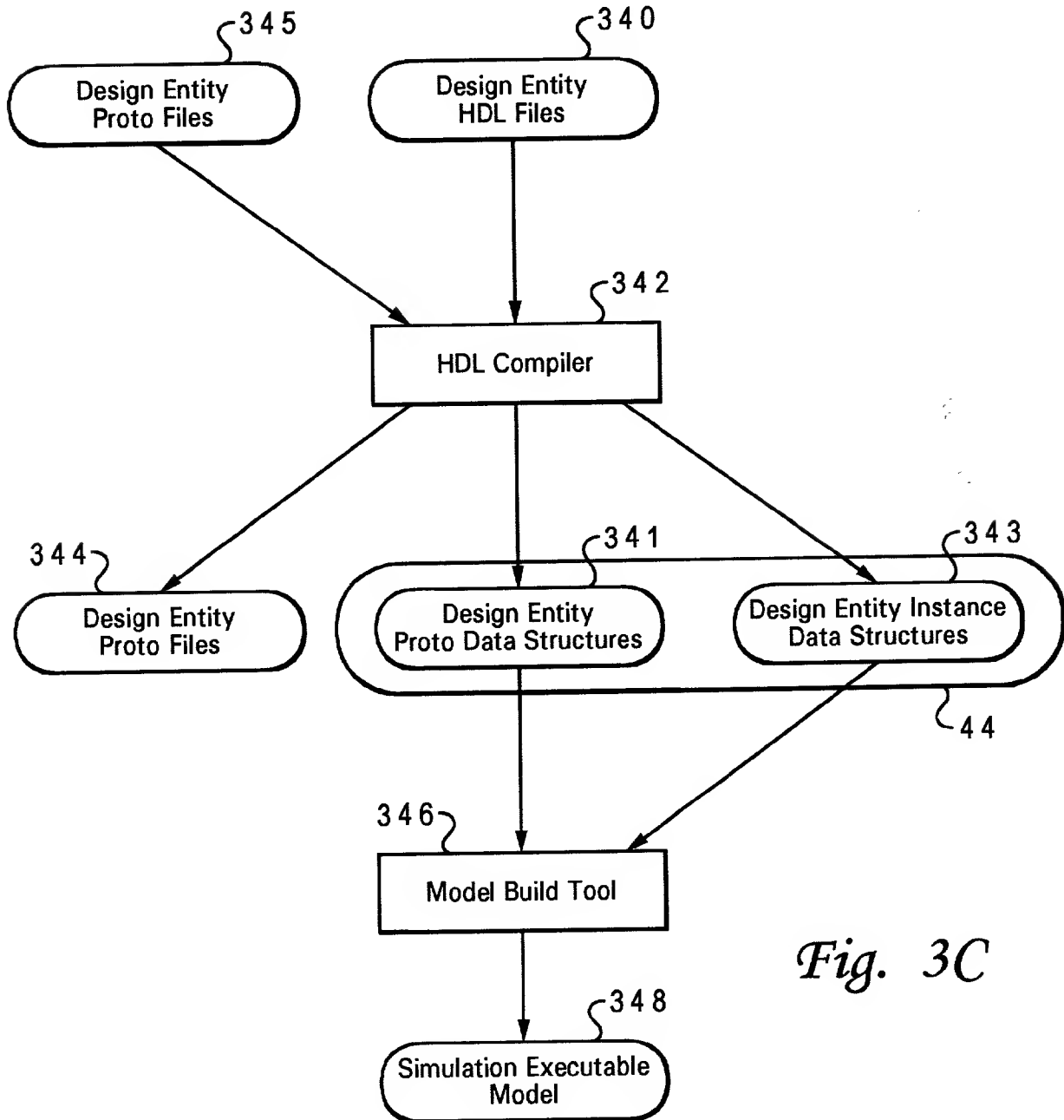


Fig. 3C

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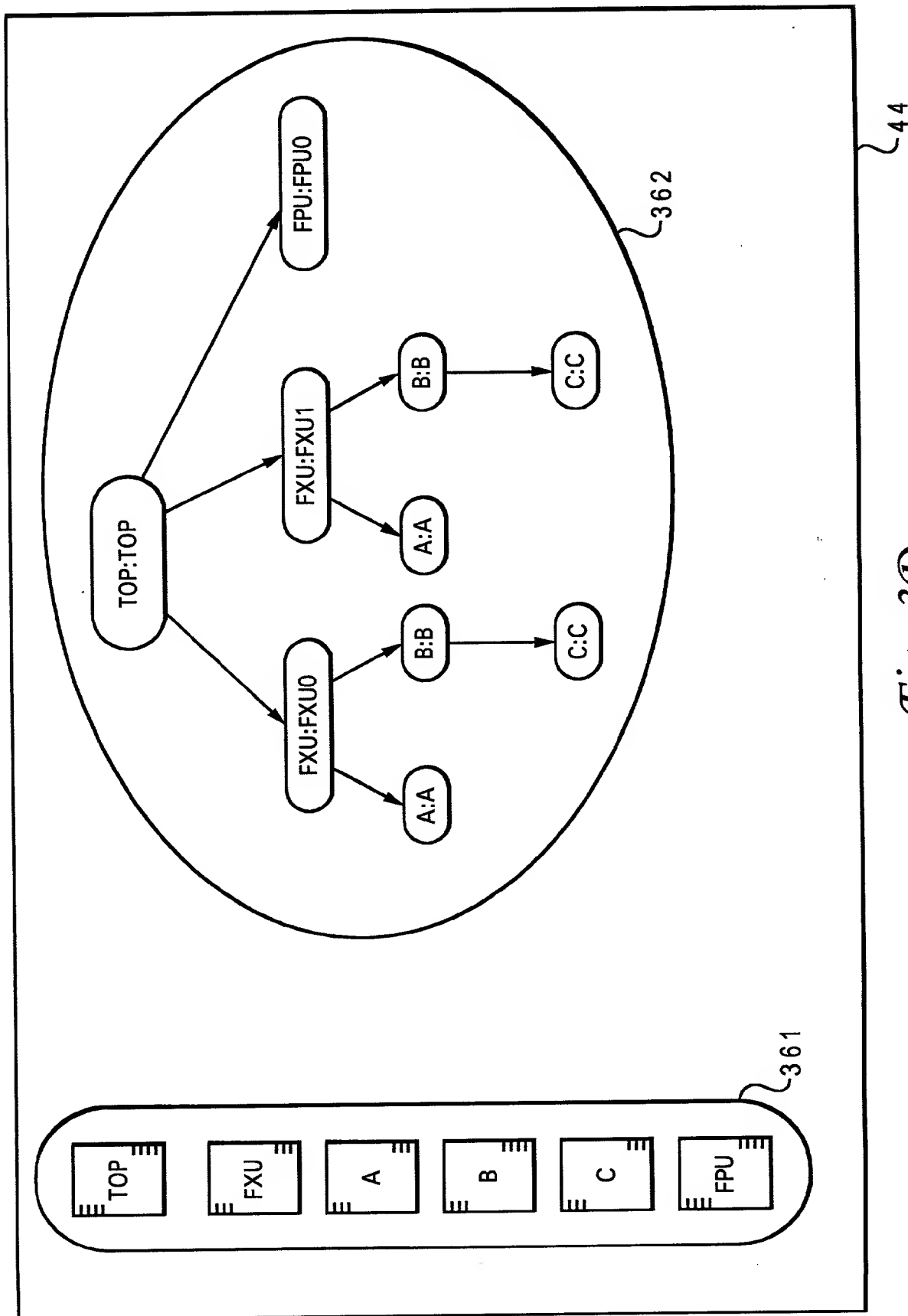


Fig. 3D

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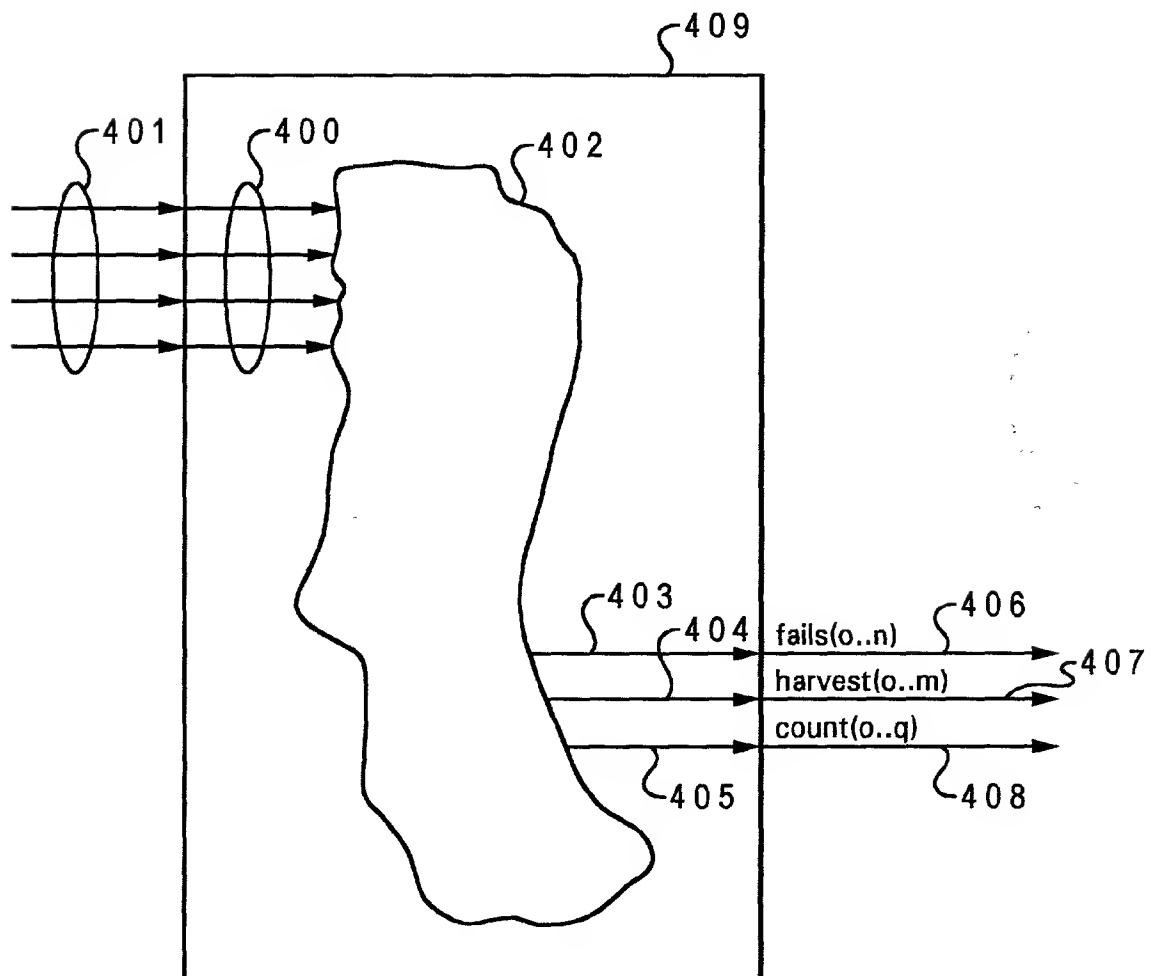


Fig. 4A

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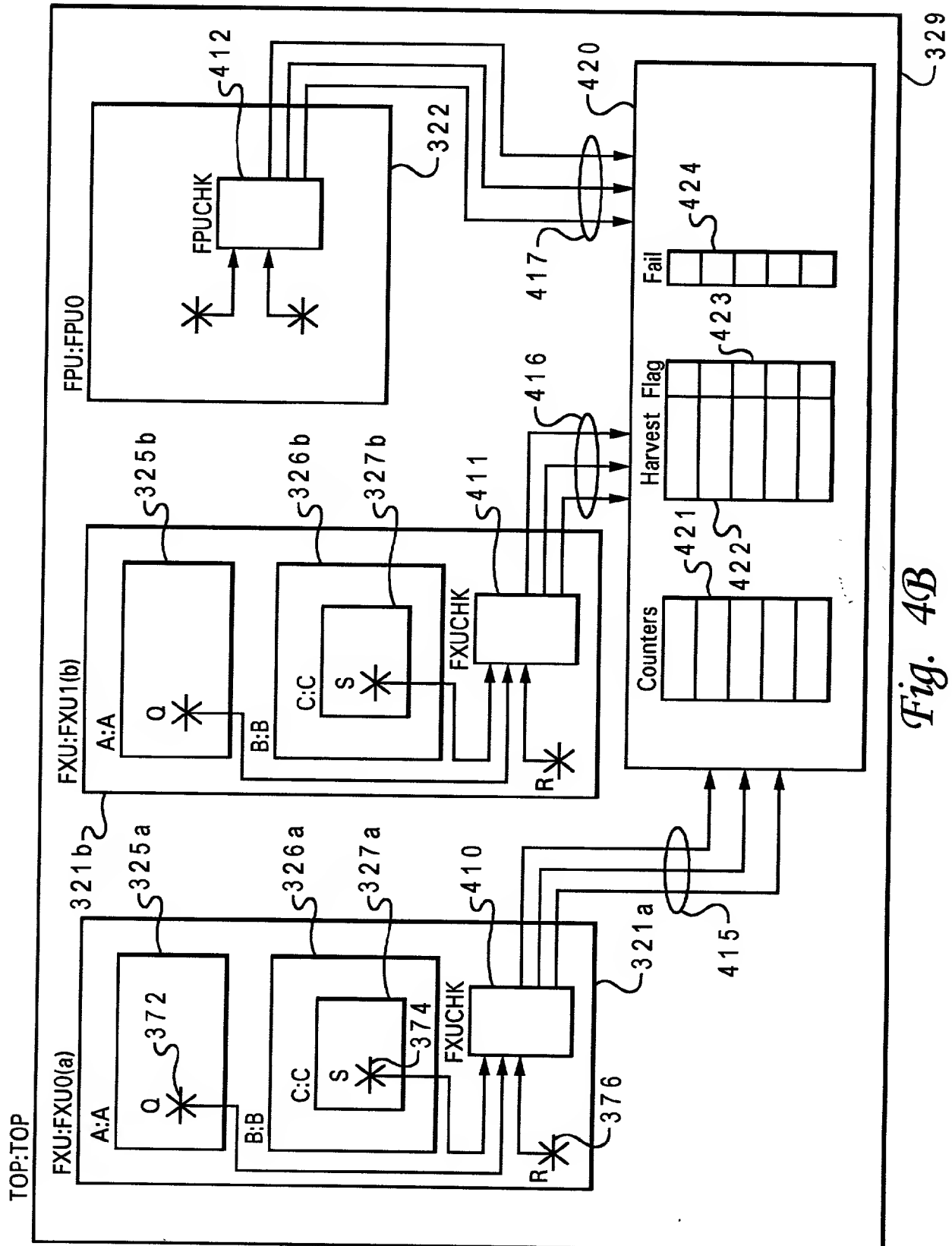


Fig. 4B

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ENTITY FXUCHK IS

```

PORT(  S_IN    :    IN std_ulogic;
        Q_IN    :    IN std_ulogic;
        R_IN    :    IN std_ulogic;
        clock   :    IN std_ulogic;
        fails   :    OUT std_ulogic_vector(0 to 1);
        counts  :    OUT std_ulogic_vector(0 to 2);
        harvests:    OUT std_ulogic_vector(0 to 1);
);

```

4 5 0

4 5 2 { --!! BEGIN
--!! Design Entity: FXU;

4 5 3 { --!! Inputs
--!! S_IN => B.C.S;
--!! Q_IN => A.Q;
--!! R_IN => R;
--!! CLOCK => clock;
--!! End Inputs

4 5 4 { --!! Fail Outputs;
--!! 0 : "Fail message for failure event 0";
--!! 1 : "Fail message for failure event 1";
--!! End Fail Outputs;

4 5 1

4 5 5 { --!! Count Outputs;
--!! 0 : <event0> clock;
--!! 1 : <event1> clock;
--!! 2 : <event2> clock;
--!! End Count Outputs;

4 5 6 { --!! Harvest Outputs;
--!! 0 : "Message for harvest event 0";
--!! 1 : "Message for harvest event 1";
--!! End Harvest Outputs;

4 5 7 { --!! End;

4 4 0

ARCHITECTURE example of FXUCHK IS

BEGIN

... HDL code for entity body section ...

END;

4 5 8

Fig. 4C

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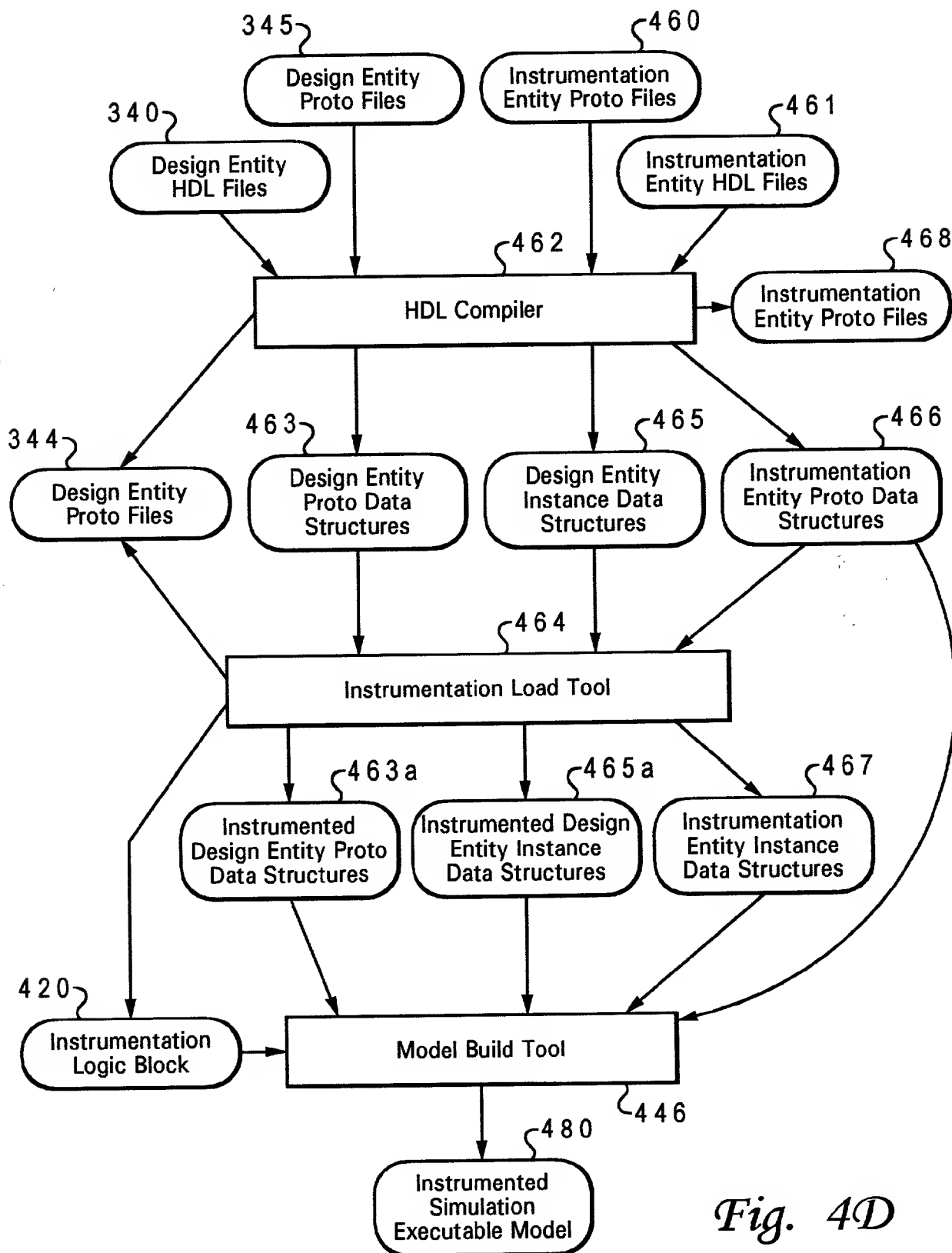
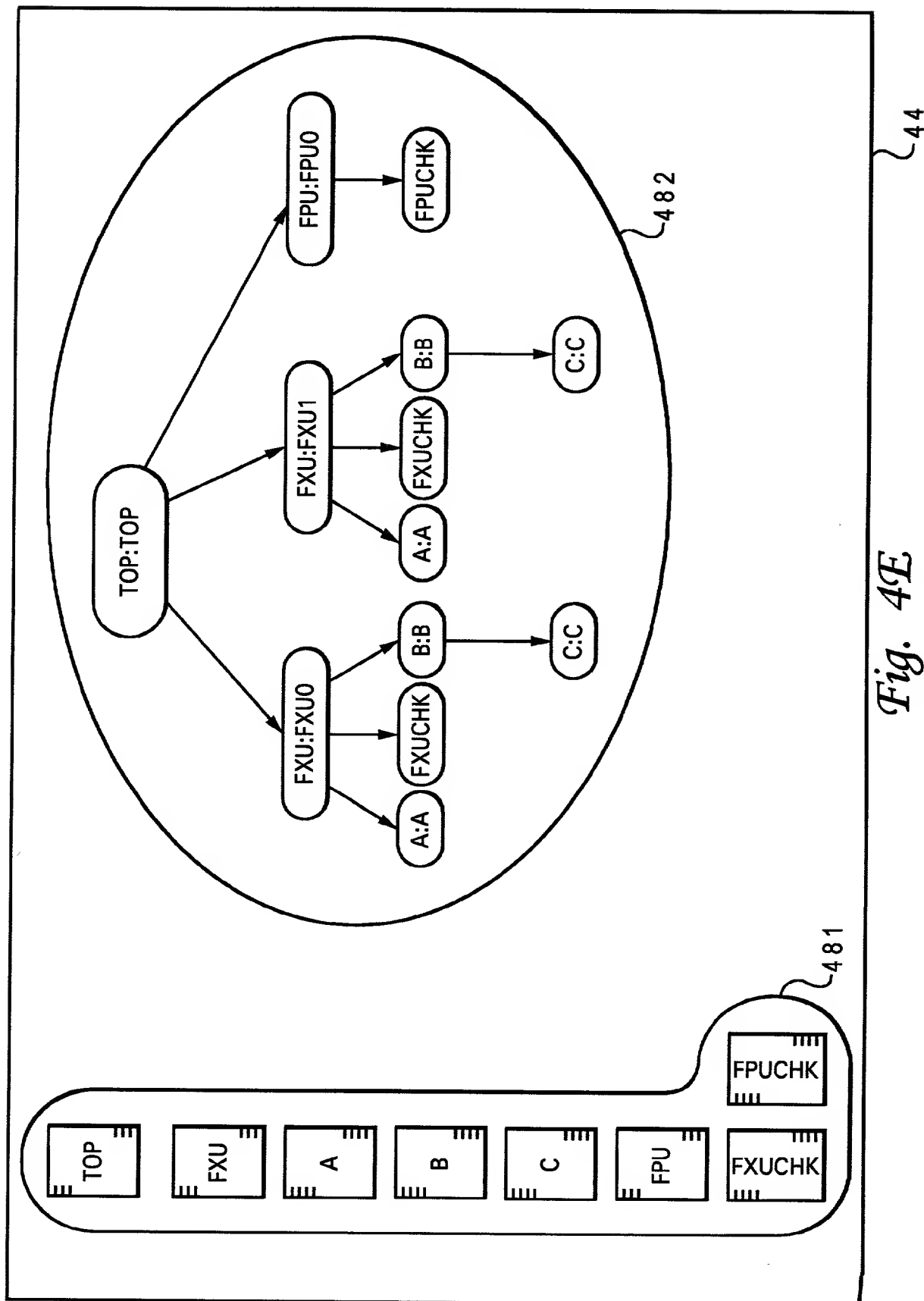


Fig. 4D



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Fig. 5A

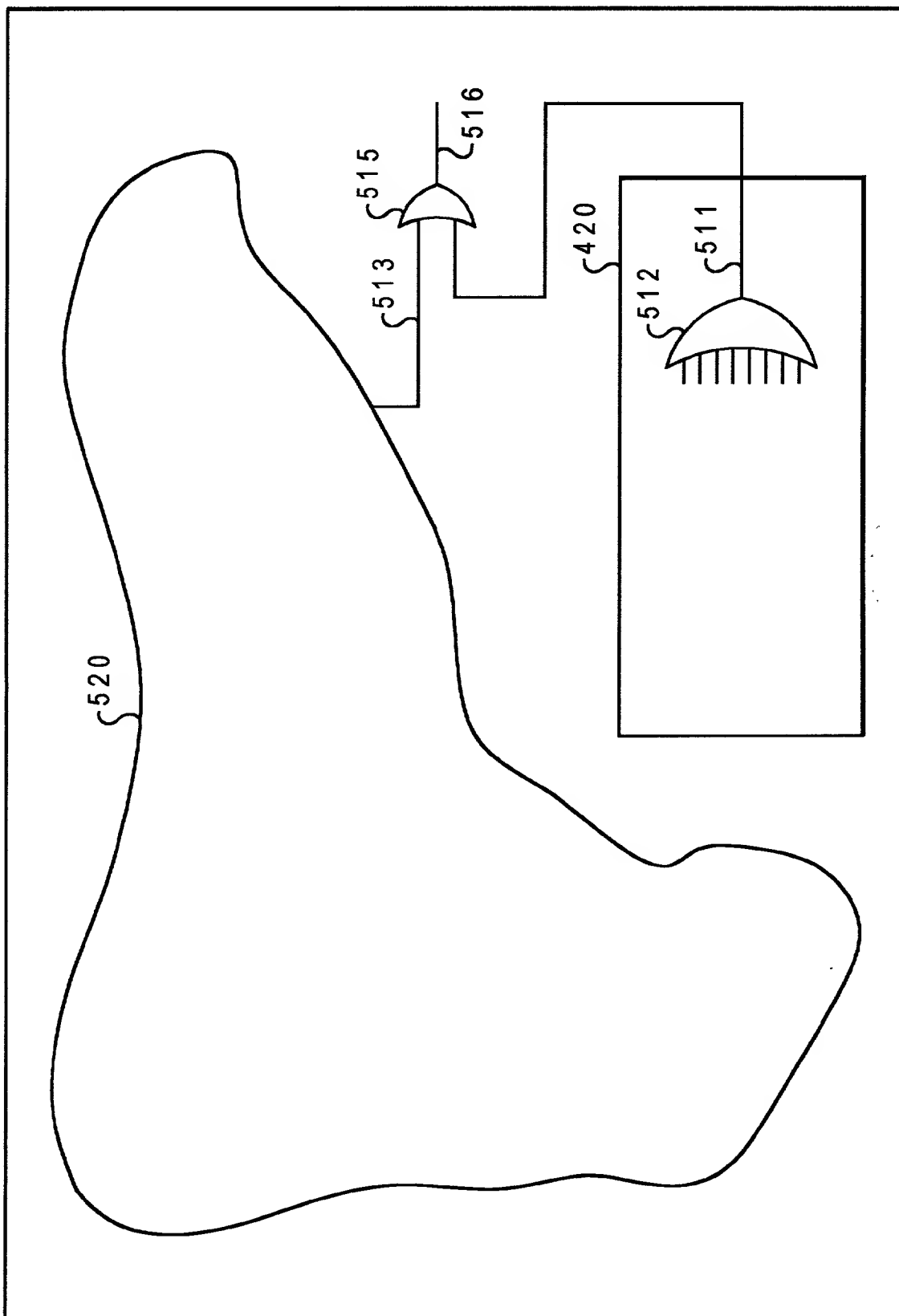


Fig. 5B

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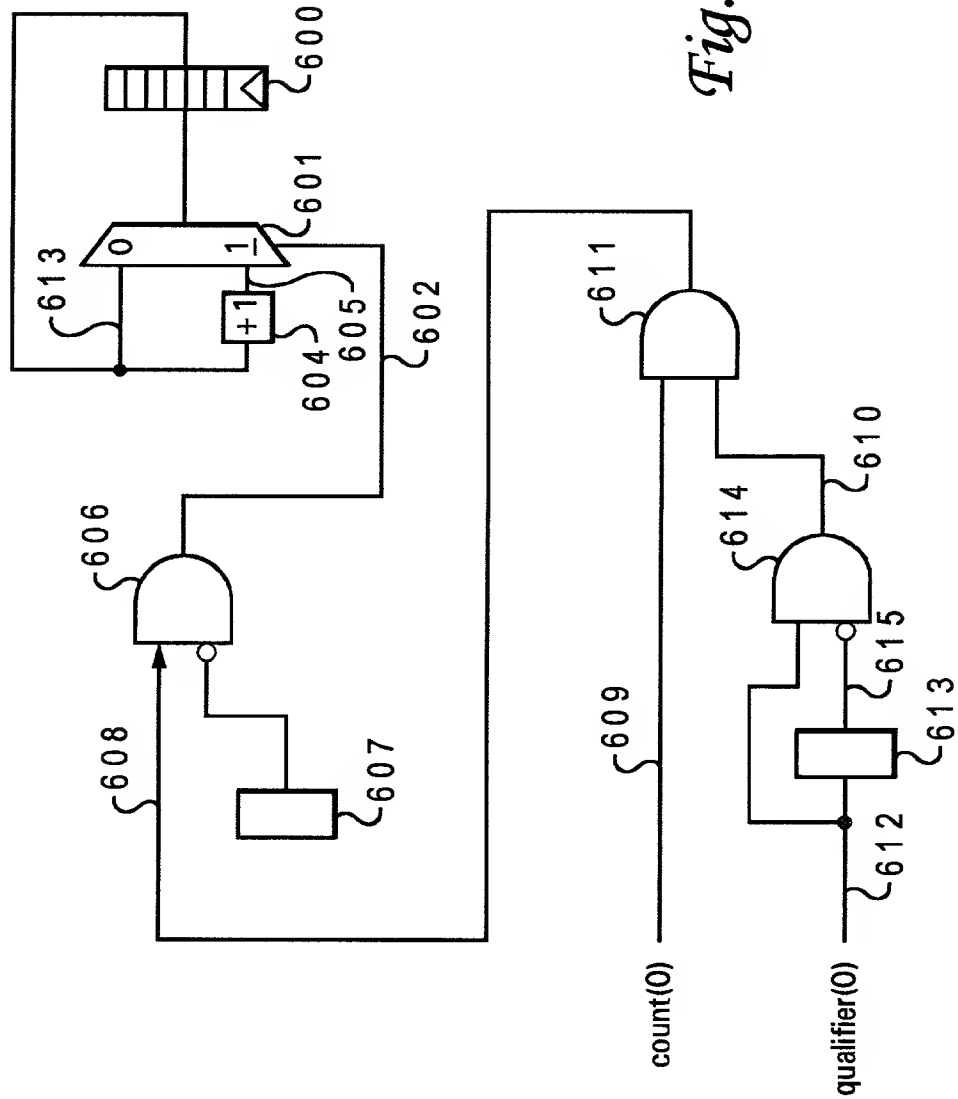


Fig. 6A

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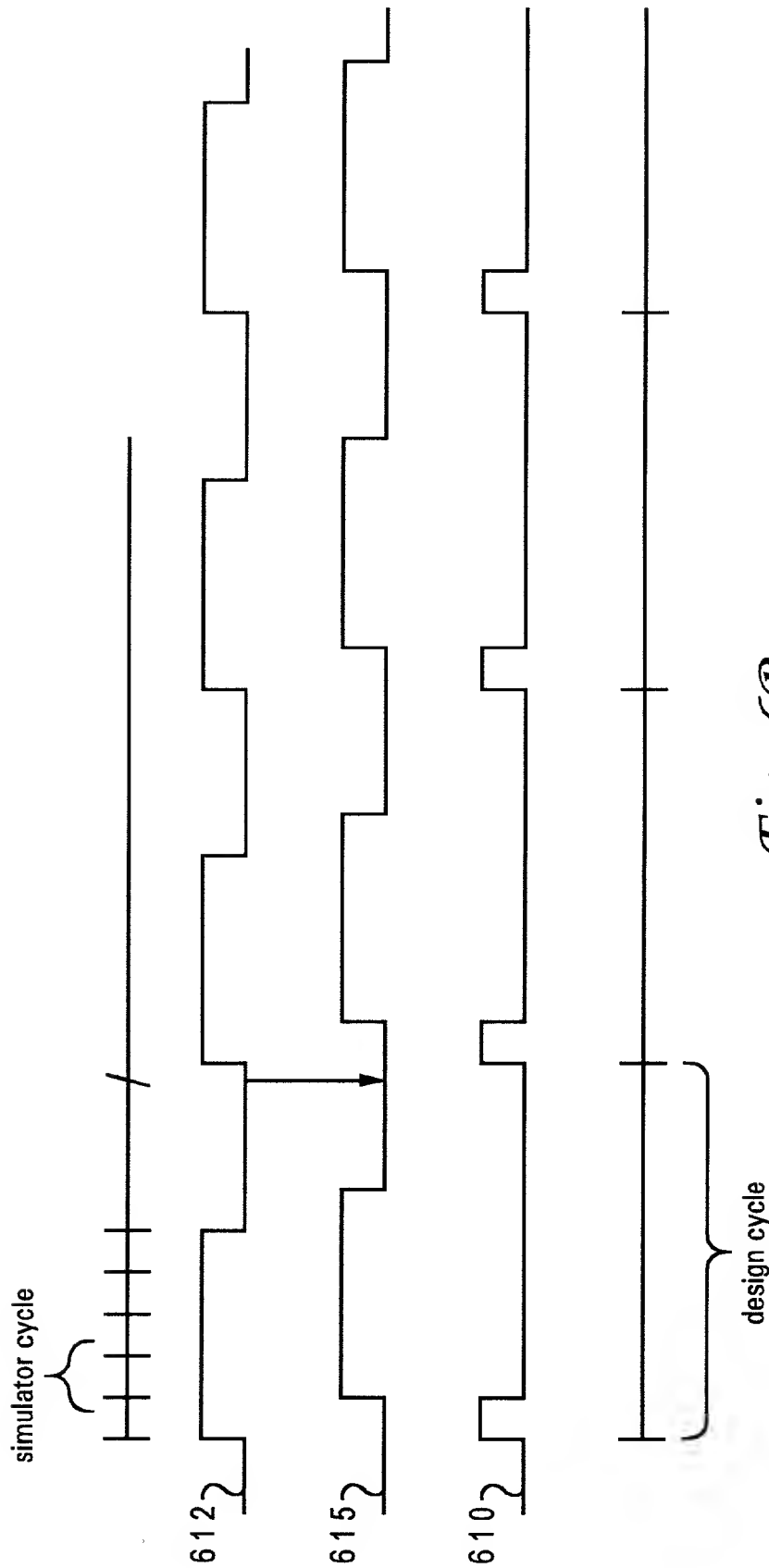


Fig. 6B

2030000651US1

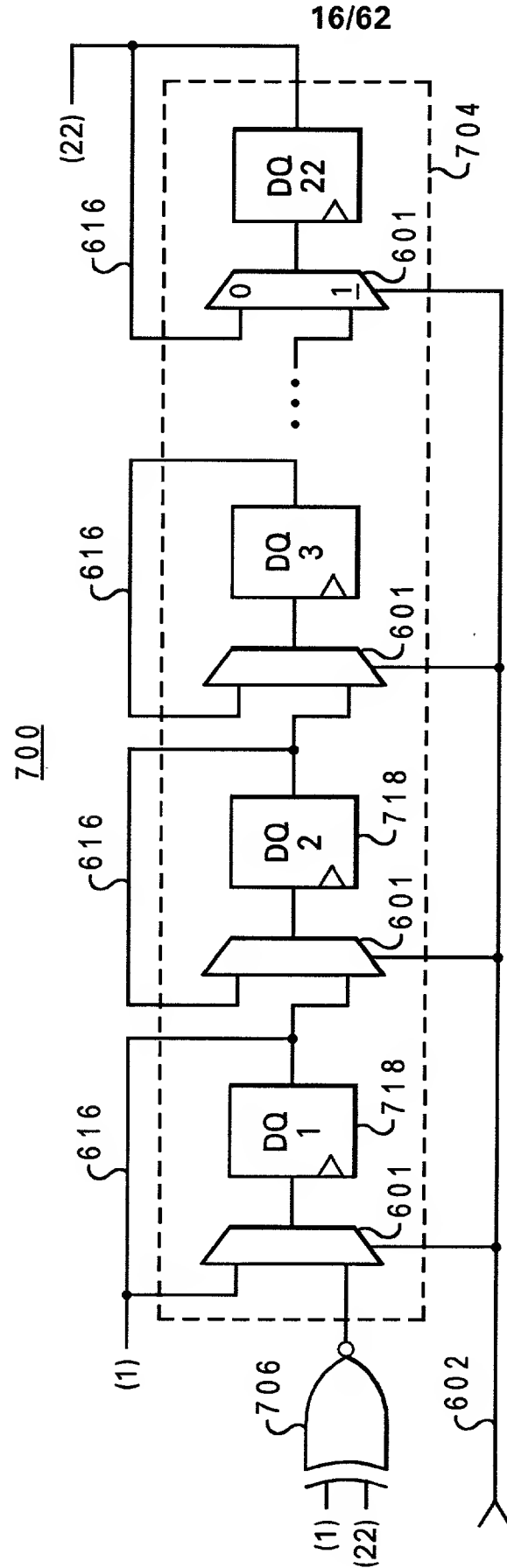


Fig. 7



Prior Art

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entity FSM : FSM

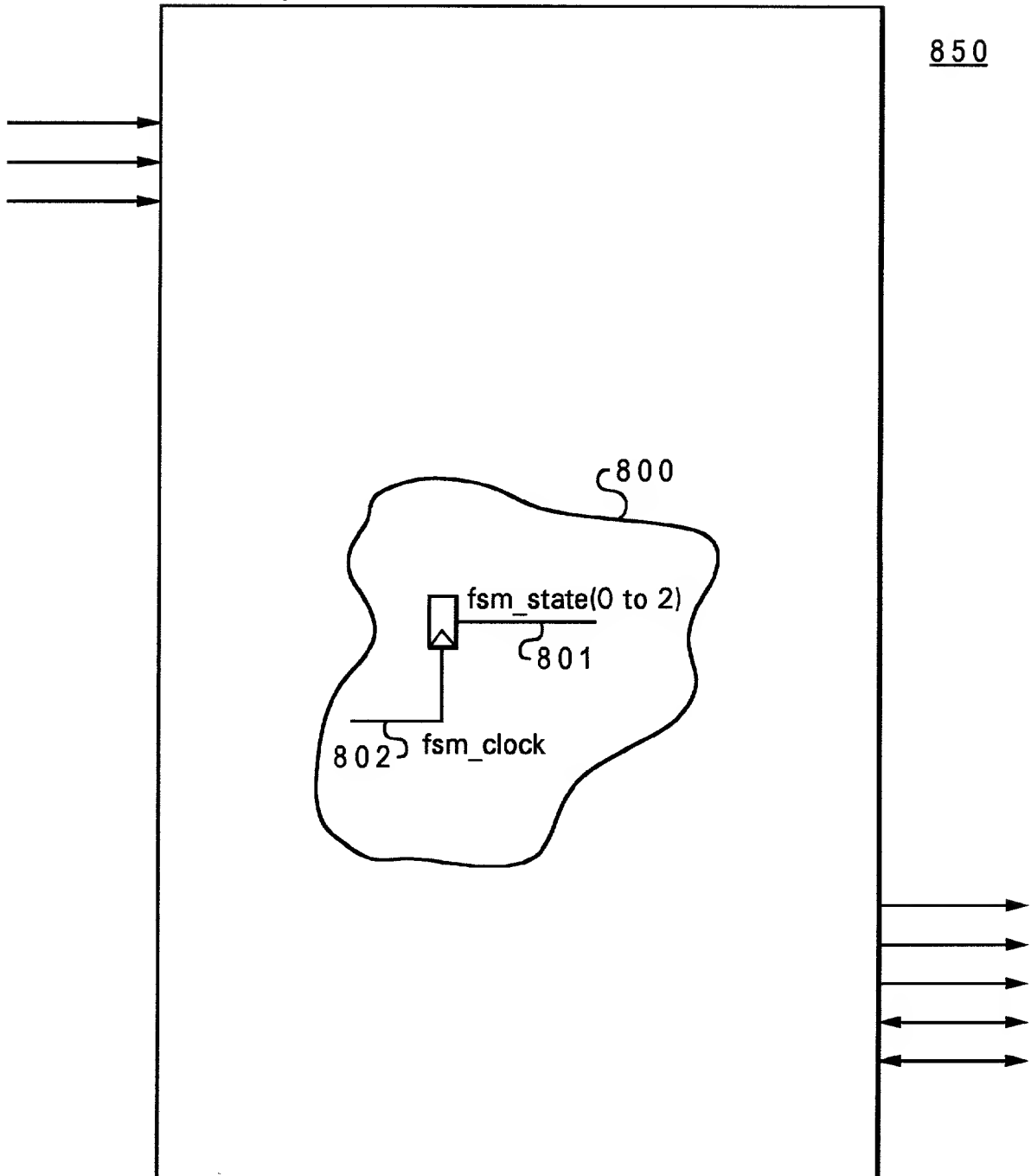


Fig. 8B
Prior Art

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ENTITY FSM IS

PORT(
....ports for entity fsm....
);

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

fsm_state(0 to 2) <= ... Signal 801 ...

8 5 3	{	--!! Embedded FSM : examplefsm;	}	8 5 2	}	8 6 0
8 5 9	{	--!! clock : (fsm_clock);				
8 5 4	{	--!! state_vector : (fsm_state(0 to 2));				
8 5 5	{	--!! states : (S0, S1, S2, S3, S4);				
8 5 6	{	--!! state_encoding : ('000', '001', '010', '011', '100');				
	{	--!! arcs : (S0 => S0, S0 => S1, S0 => S2,				
8 5 7	{	--!! (S1 => S2, S1 => S3, S2 => S2,				
	{	--!! (S2 => S3, S3 => S4, S4 => S0);				
8 5 8	{	--!! End FSM;				

END;

Fig. 8C

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entity FSM : FSM

850

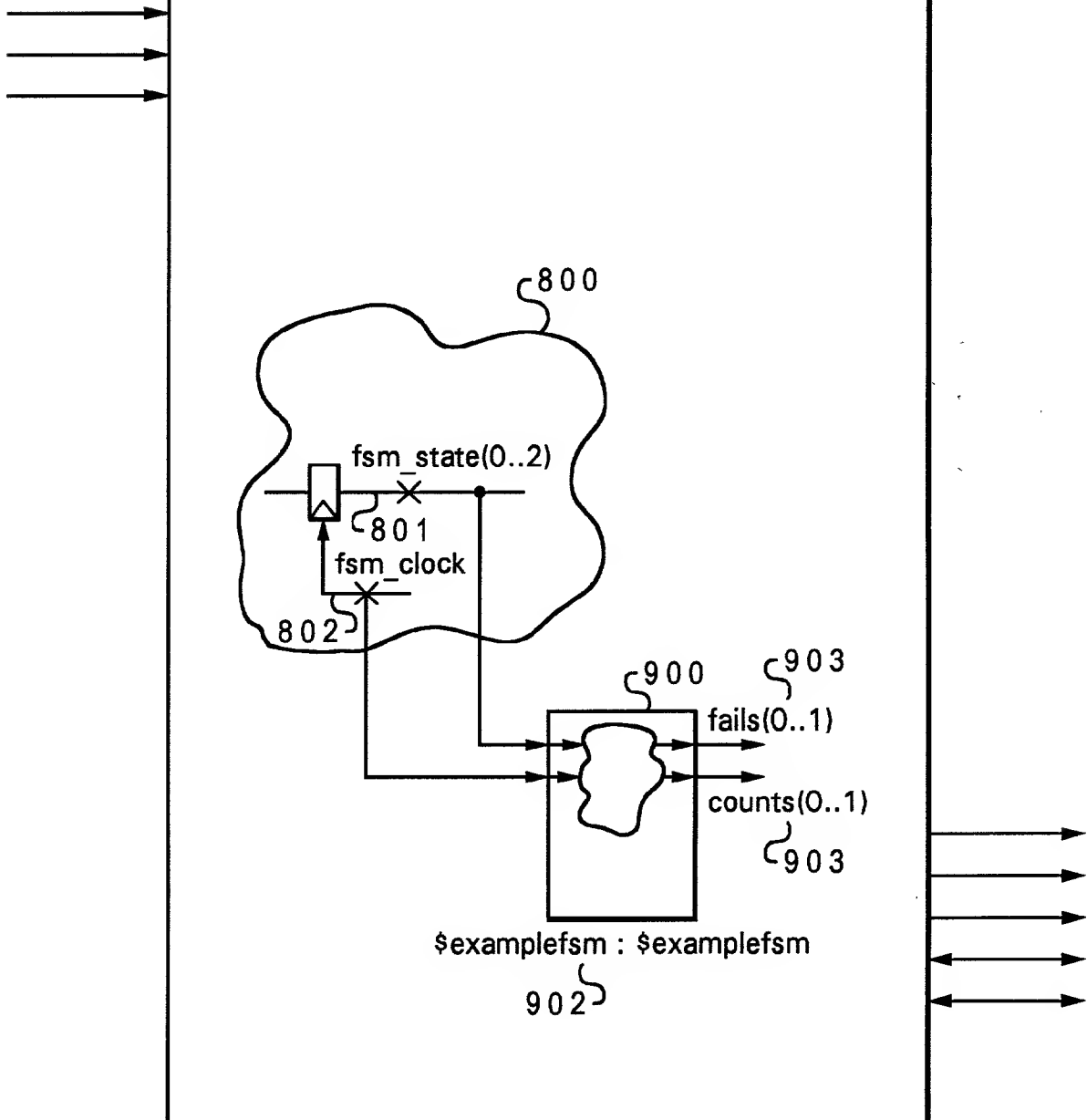
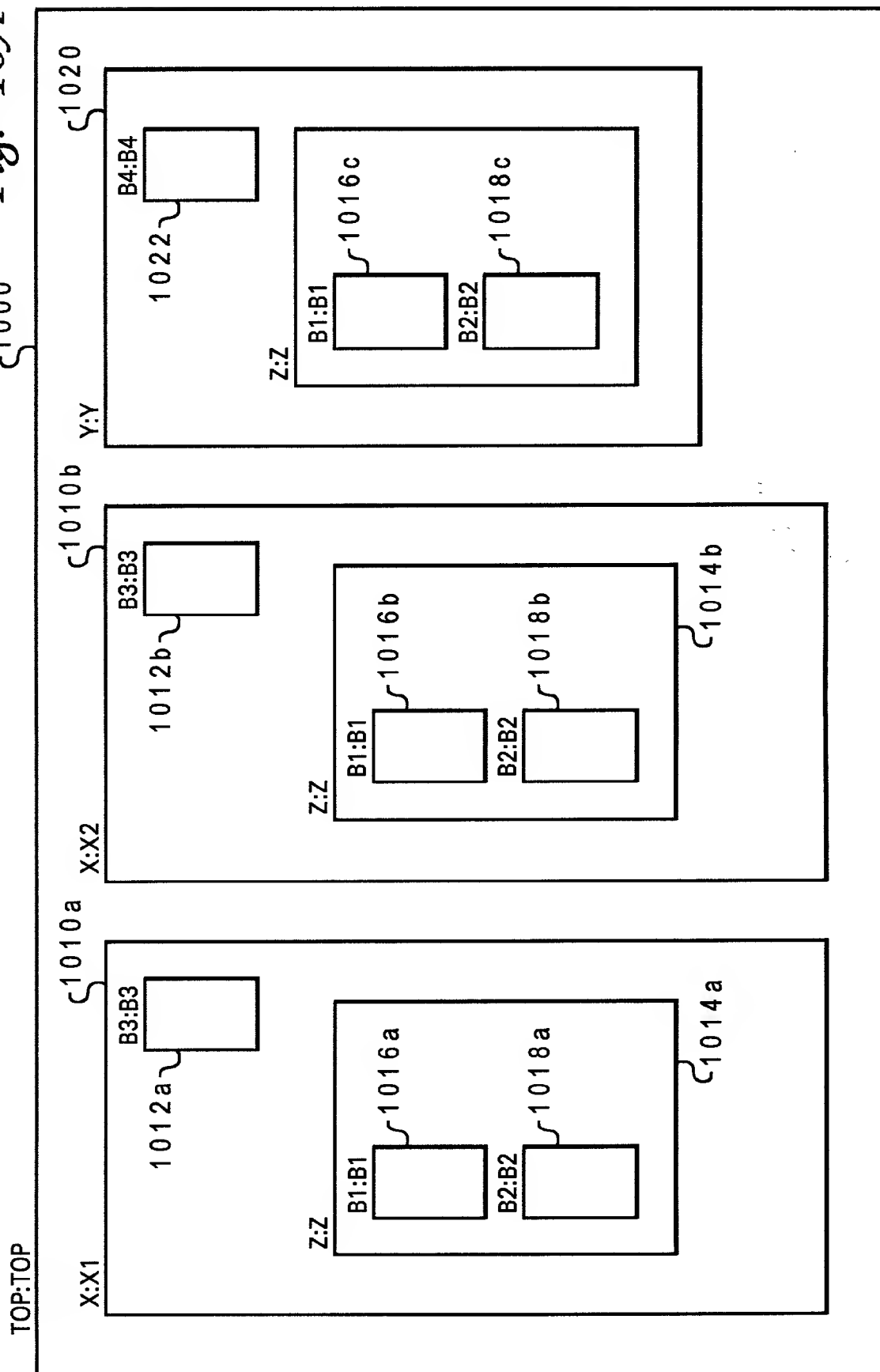


Fig. 9

Fig. 10A



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1030
<instantiation identifier> . <instrumentation entity name> . <design entity name> . <eventname>
1032
1034
1036

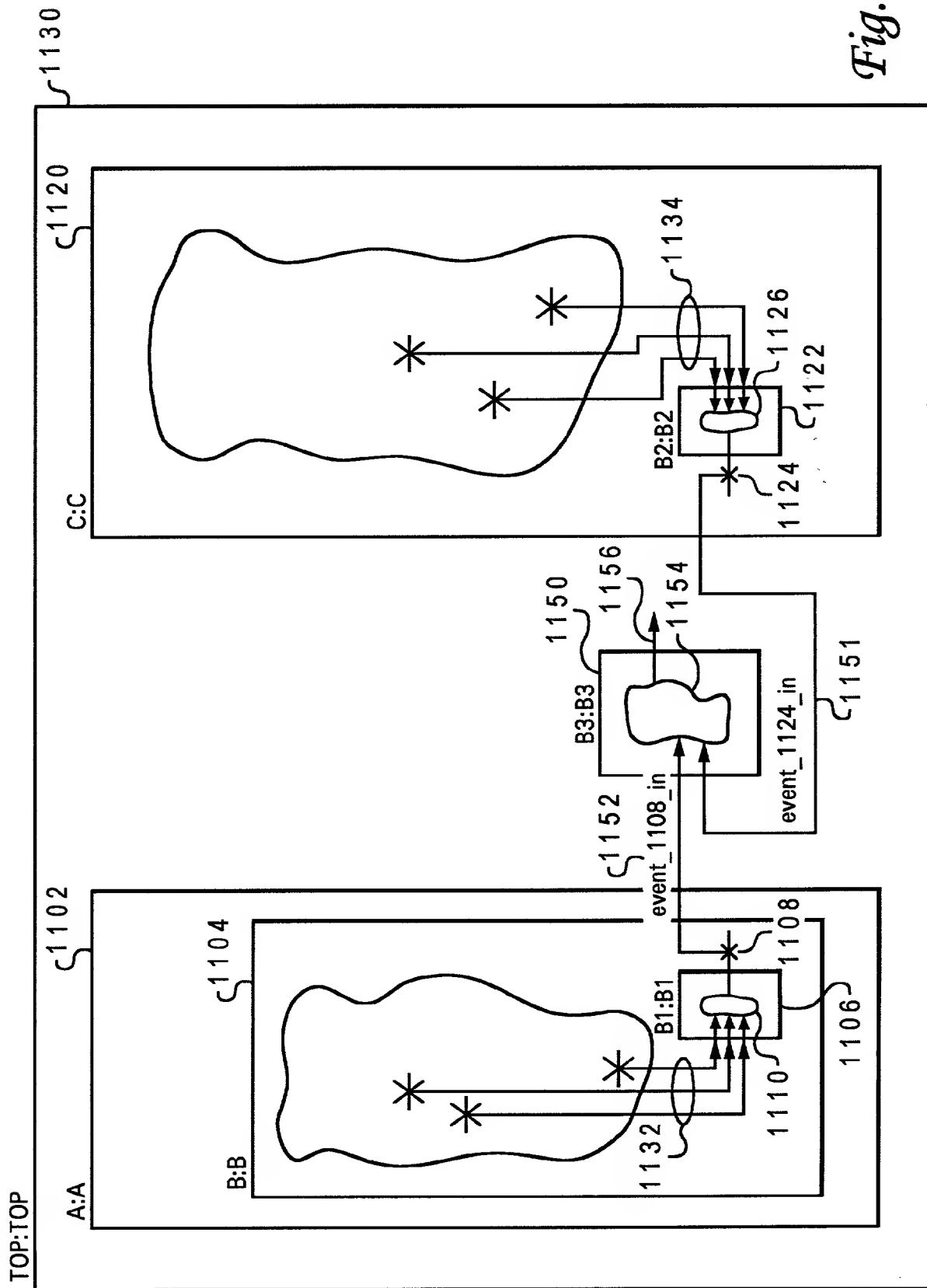
Fig. 10B

1030	1032	1034	1036
X1	B3	X	COUNT1
X1.Z	B1	Z	COUNT1
X1.Z	B2	Z	COUNT1
X2	B3	X	COUNT1
X2.Z	B1	Z	COUNT1
X2.Z	B2	Z	COUNT1
Y	B4	Y	COUNT1
Y.Z	B1	Z	COUNT1
Y.Z	B2	Z	COUNT1
			1040
			1041
			1042
			1043
			1044
			1045
			1046
			1047
			1048

Fig. 10C

1030
<instantiation identifier> . <design entity name> . <eventname>
1034
1036

Fig. 10D



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--!! Inputs
--!! event_1108_in <= C.[B2.count.event_1108];
--!! event_1124_in <= A.B.[B1.count.event_1124];
--!! End Inputs

1163 1165 1161 1162 1164 1166

The diagram shows two event lines. The first line is 'event_1108_in <= C.[B2.count.event_1108];' with a bracket above it labeled '1163' and a bracket below it labeled '1164'. The second line is 'event_1124_in <= A.B.[B1.count.event_1124];' with a bracket above it labeled '1165' and a bracket below it labeled '1166'. To the right of the first line is a bracket labeled '1161' and to the right of the second line is a bracket labeled '1162'.

Fig. 11B

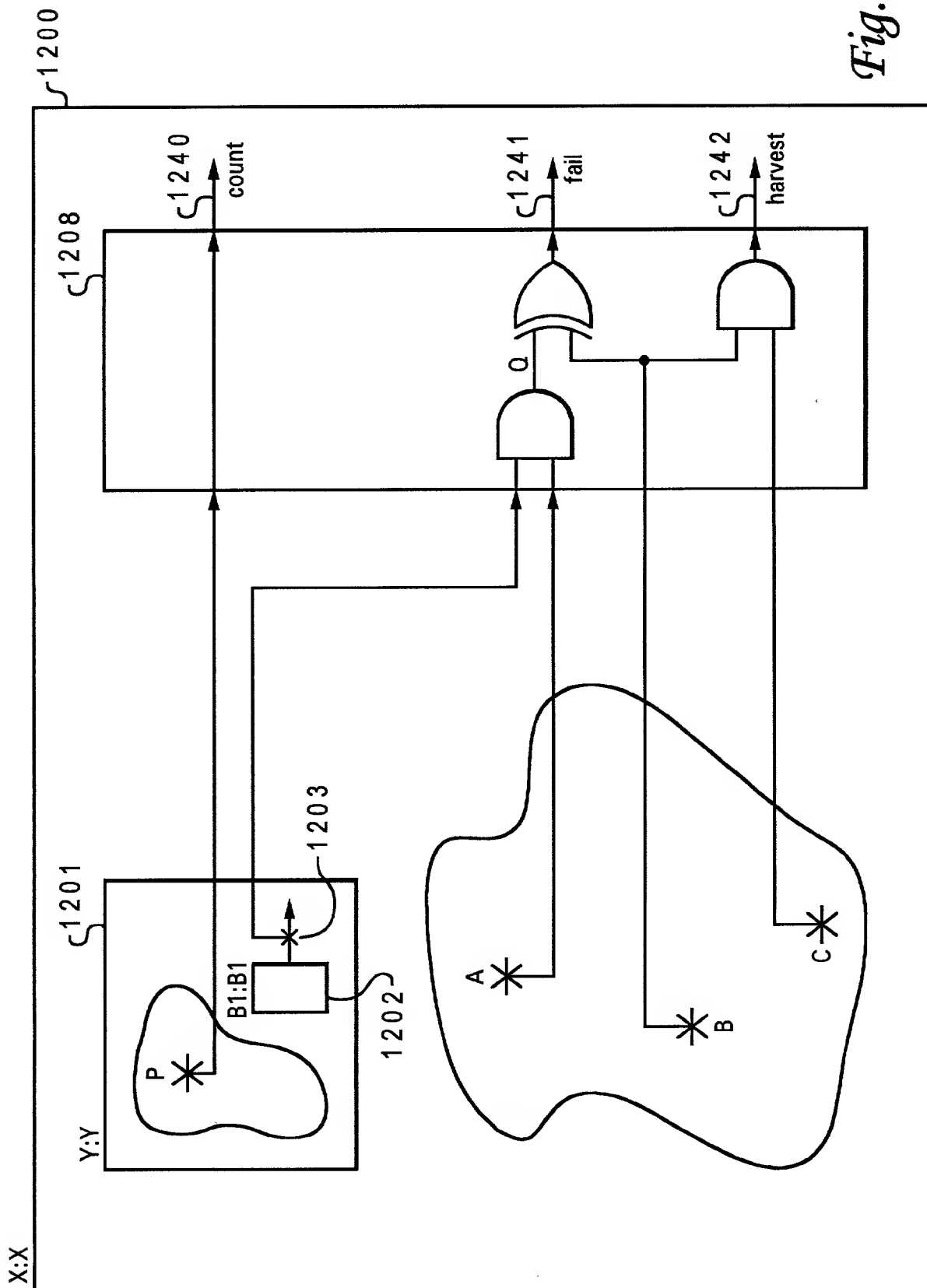
--!! Inputs
--!! event_1108_in <= C.[count.event_1108];
--!! event_1124_in <= B.[count.event_1124];
--!! End Inputs

1171 1172

The diagram shows two event lines. The first line is 'event_1108_in <= C.[count.event_1108];' with a bracket above it labeled '1171'. The second line is 'event_1124_in <= B.[count.event_1124];' with a bracket above it labeled '1172'.

Fig. 11C

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1

Fig. 12B

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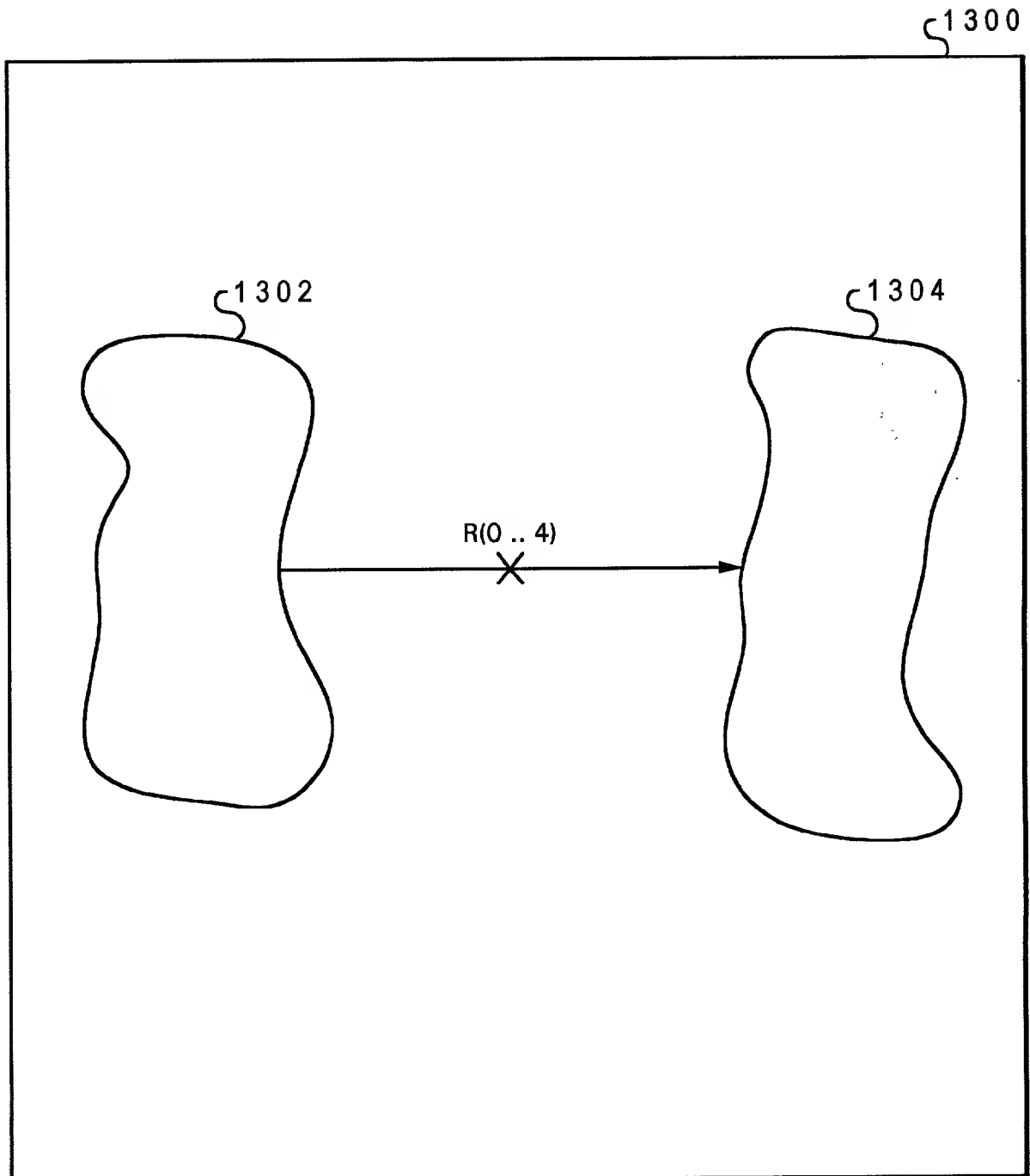
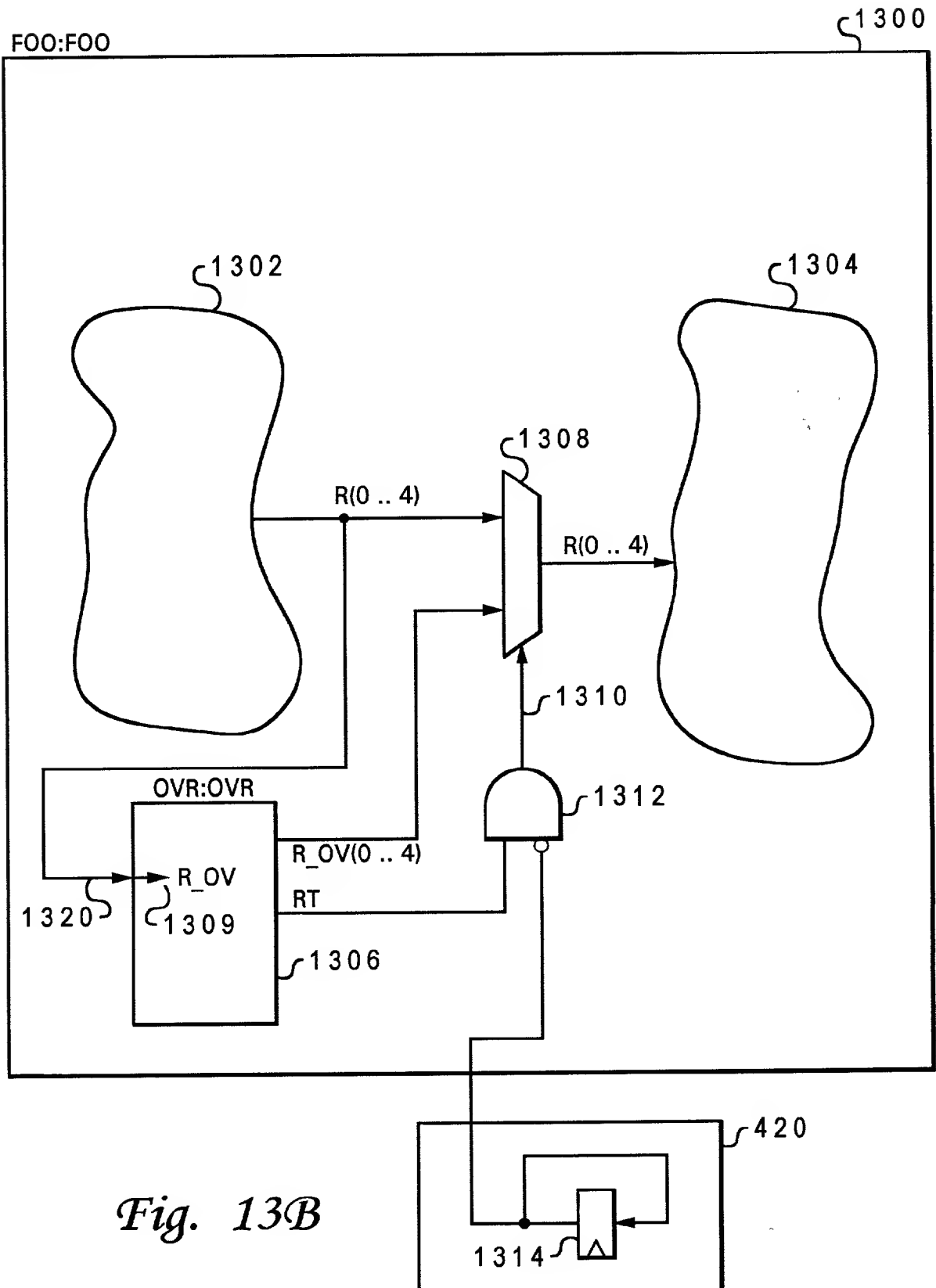


Fig. 13A

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ENTITY OVR IS

PORT(R_IN : IN std_ulogic_vector(0 .. 4);
.
.
... other ports as required ...
.
.
R_OV : OUT std_ulogic_vector(0 .. 4);
RT : OUT std_ulogic
);

--!! BEGIN
--!! Design Entity: FOO;

--!! Inputs (0 to 4)
--!! R_IN => {R(0 .. 4)};
--!! :
... other ports as needed ...
--!! :
--!! End Inputs

--!! Outputs
--!! <R_OVRRIDE> : R_OV(0 .. 4) => R(0 .. 4) [RT];
--!! End Outputs

--!! End

ARCHITECTURE example of OVR IS

BEGIN

... HDL code for entity body section ...

END;

1364
1362
1363
1360
1361
1356
1351
1340
1358

Fig. 13C

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ENTITY FOO IS

PORT(:
 :
 :
);

ARCHITECTURE example of FOO IS

BEGIN

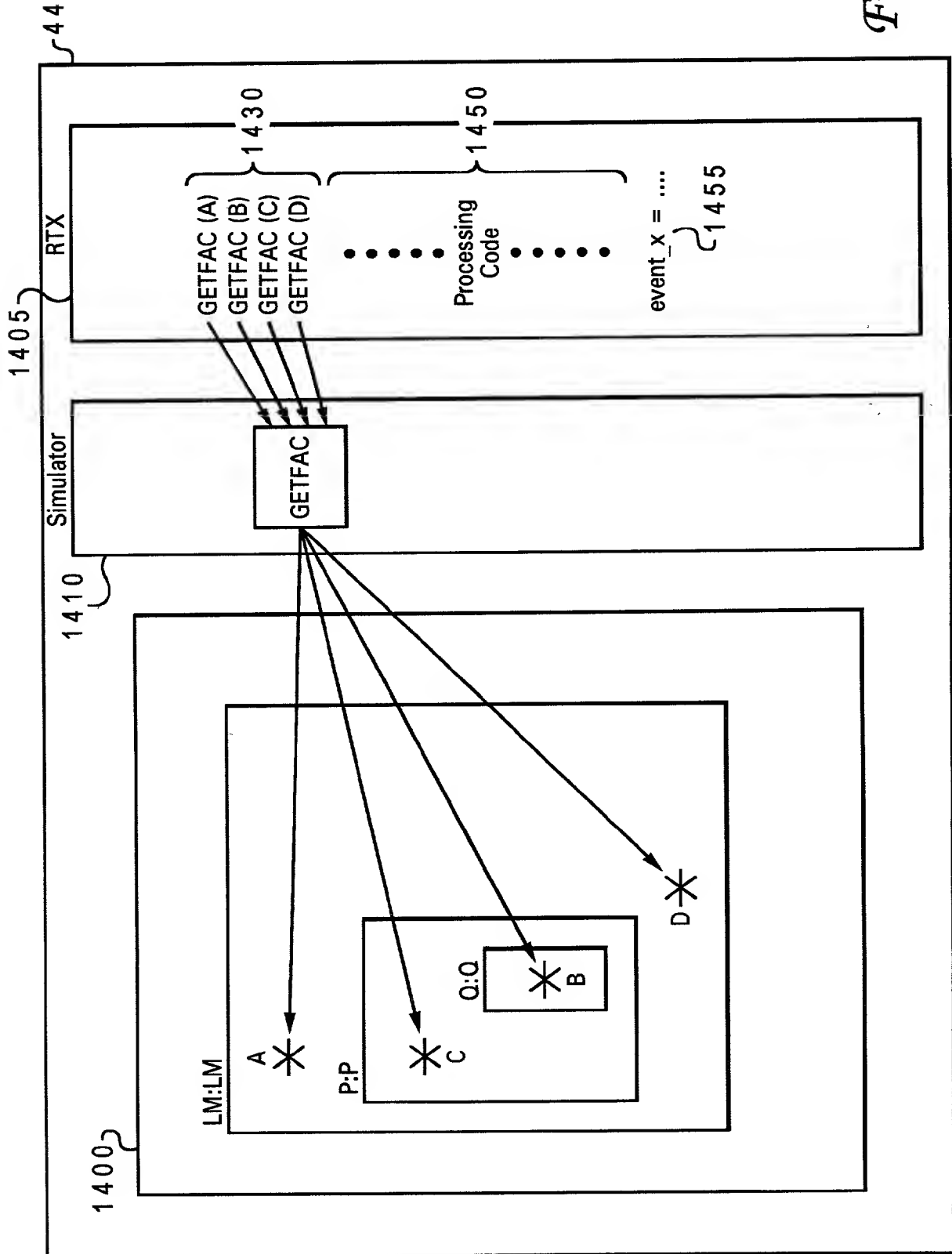
.
 .
 .
 .
 .
 R <=
 .
 .
 .
 .

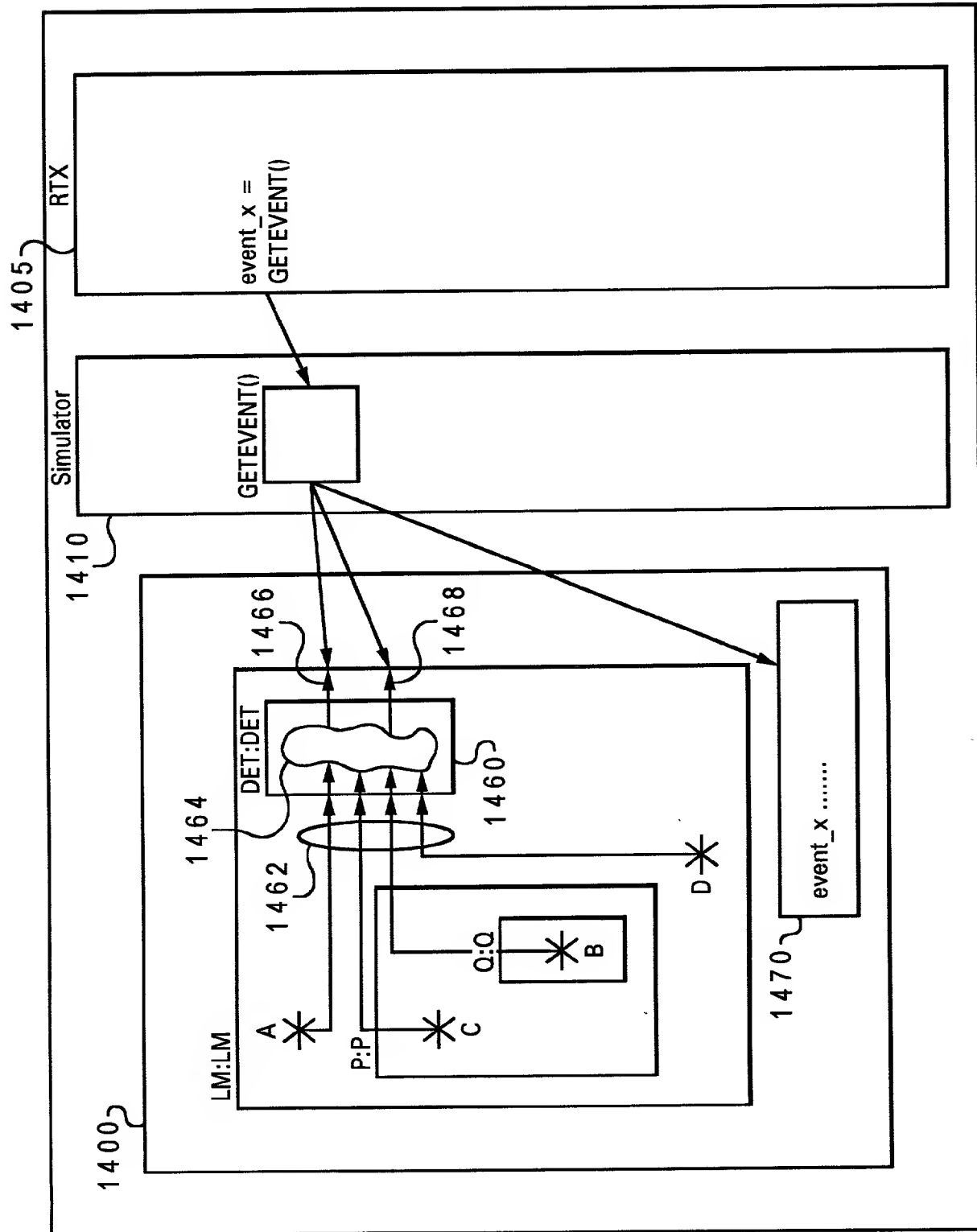
1380 { --!! R_IN <= {R}; 1381
 --!! 1382
 --!!
 --!! R_OV(0 to 4) <=; 1383
 --!! RT <=;
 --!! [override, R_OVERRIDE, R(0 .. 4), RT] <= R_OV(0 to 4);
 1384

Fig. 13D

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Fig. 14A





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```

ENTITY DET IS
    PORT(  A      :  IN std_ulogic;
           B      :  IN std_ulogic_vector(0 to 5);
           C      :  IN std_ulogic;
           D      :  IN std_ulogic;
           :
           :
           event_x :  OUT std_ulogic_vector(0 to 2);
           x_here  :  OUT std_ulogic;
    );

    --!! BEGIN
    --!! Design Entity: LM;

    --!! Inputs
    --!! A  =>  A;
    --!! B  =>  P.Q.B;
    --!! C  =>  P.C;
    --!! D  =>  D;
    --!! End Inputs

    --!! Detections
    --!! <event_x>:event_x(0 to 2) [x_here];
    --!! End Detections

    --!! End;

    ARCHITECTURE example of DET IS
    BEGIN
        ... HDL code ...

    END;

```

1491 {

1493 {

1495 {

1494 {

1480 {

1492 {

Fig. 14C

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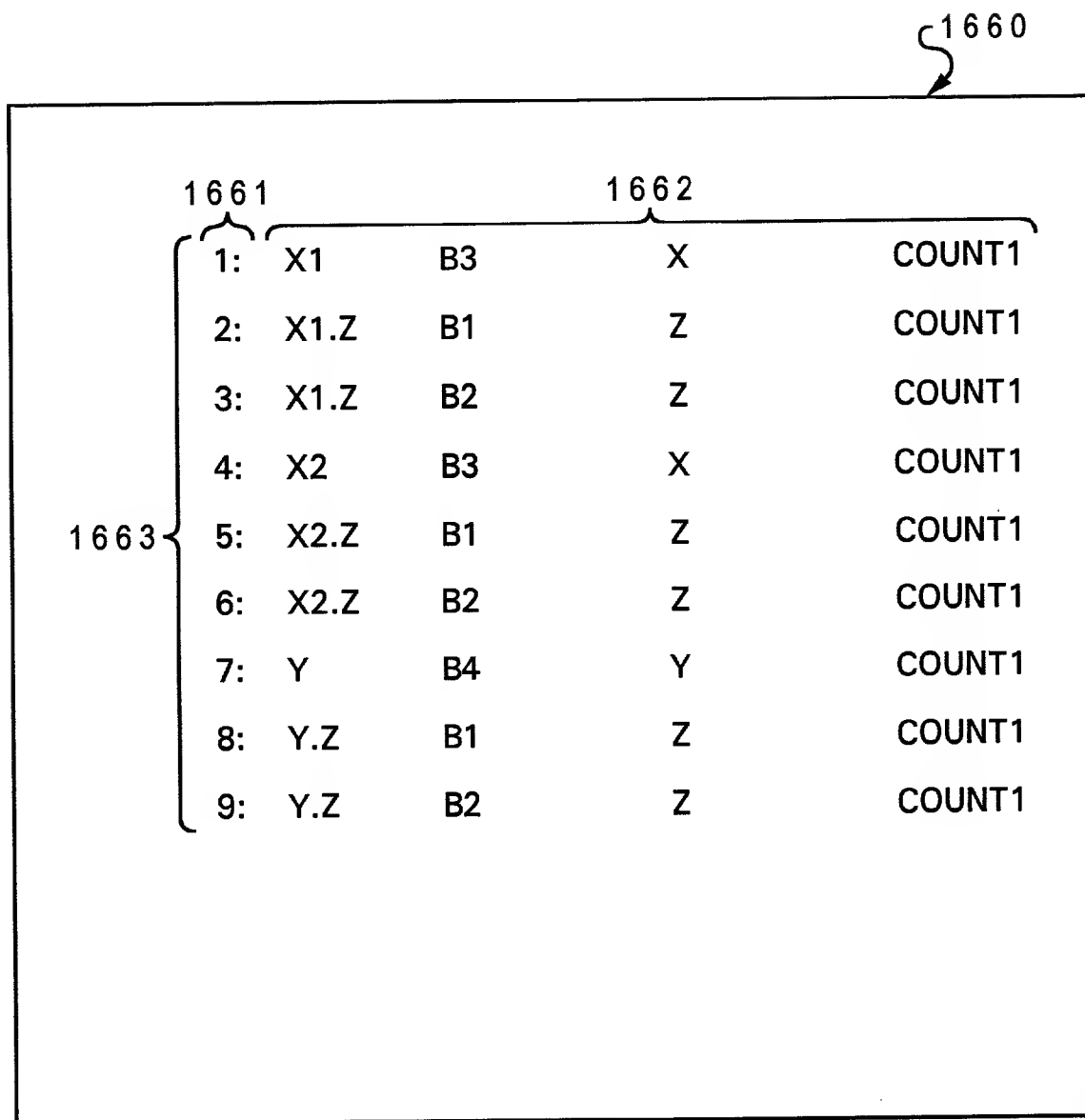
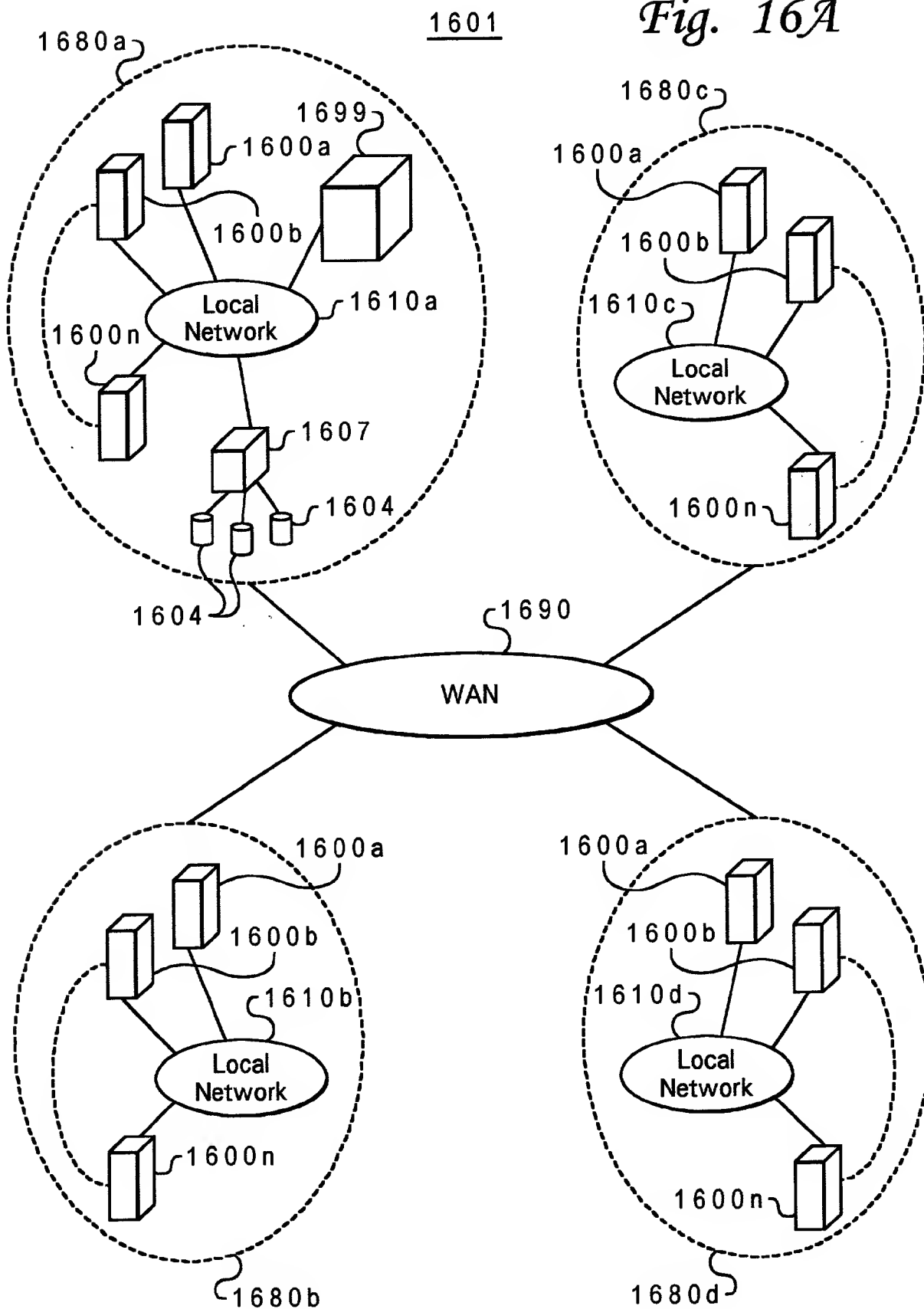


Fig. 15

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Fig. 16A



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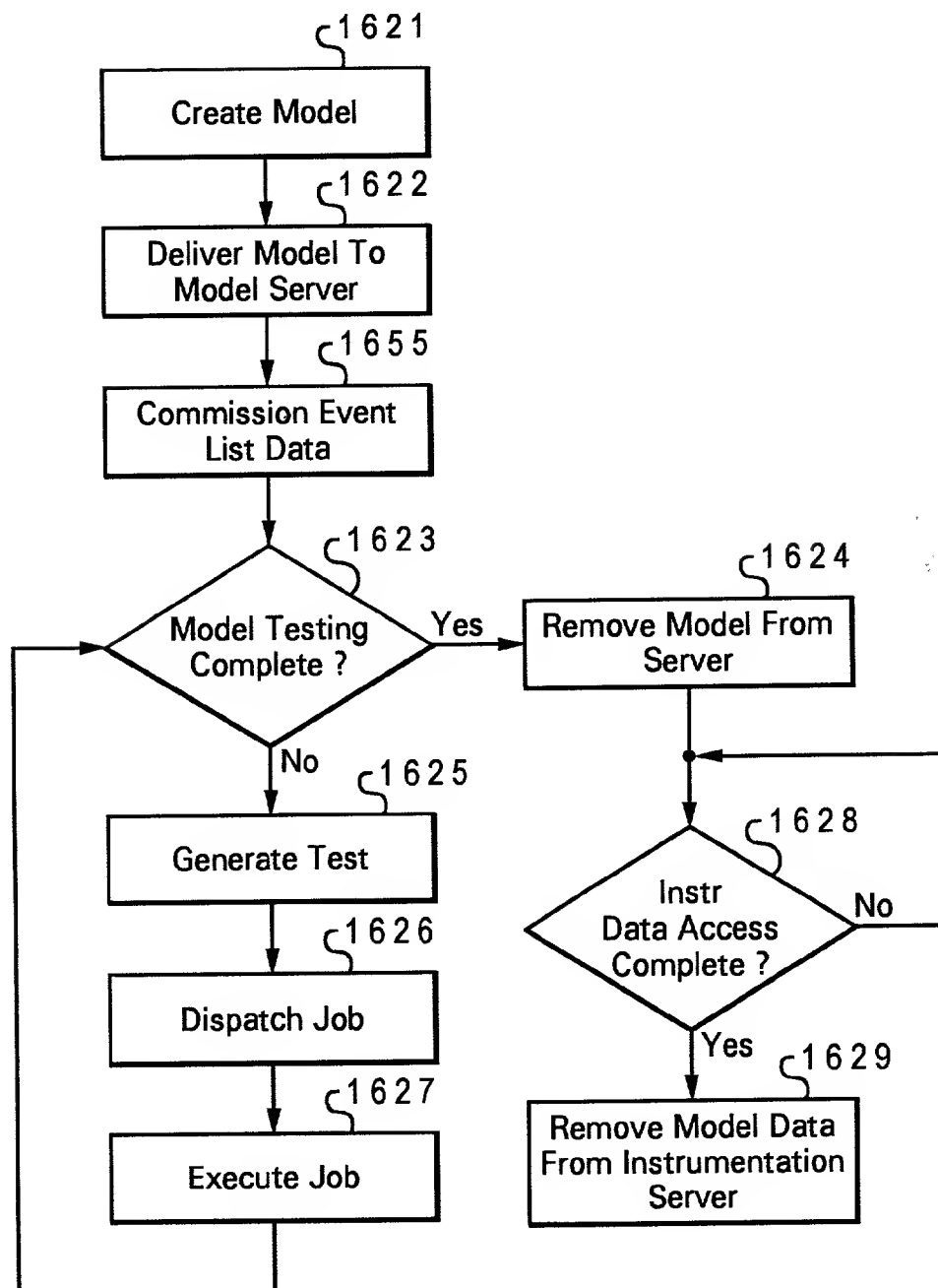


Fig. 16B

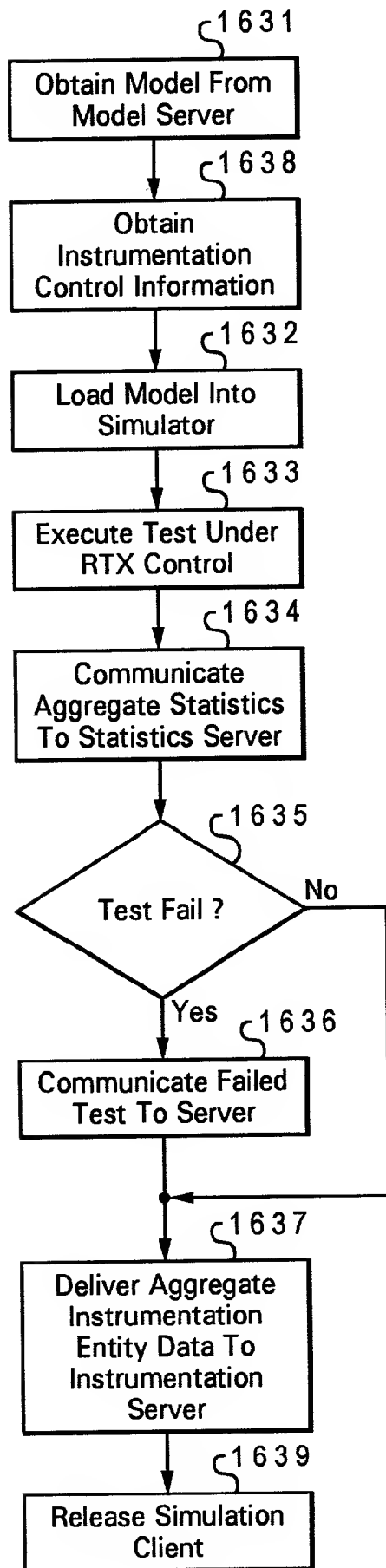


Fig. 16C

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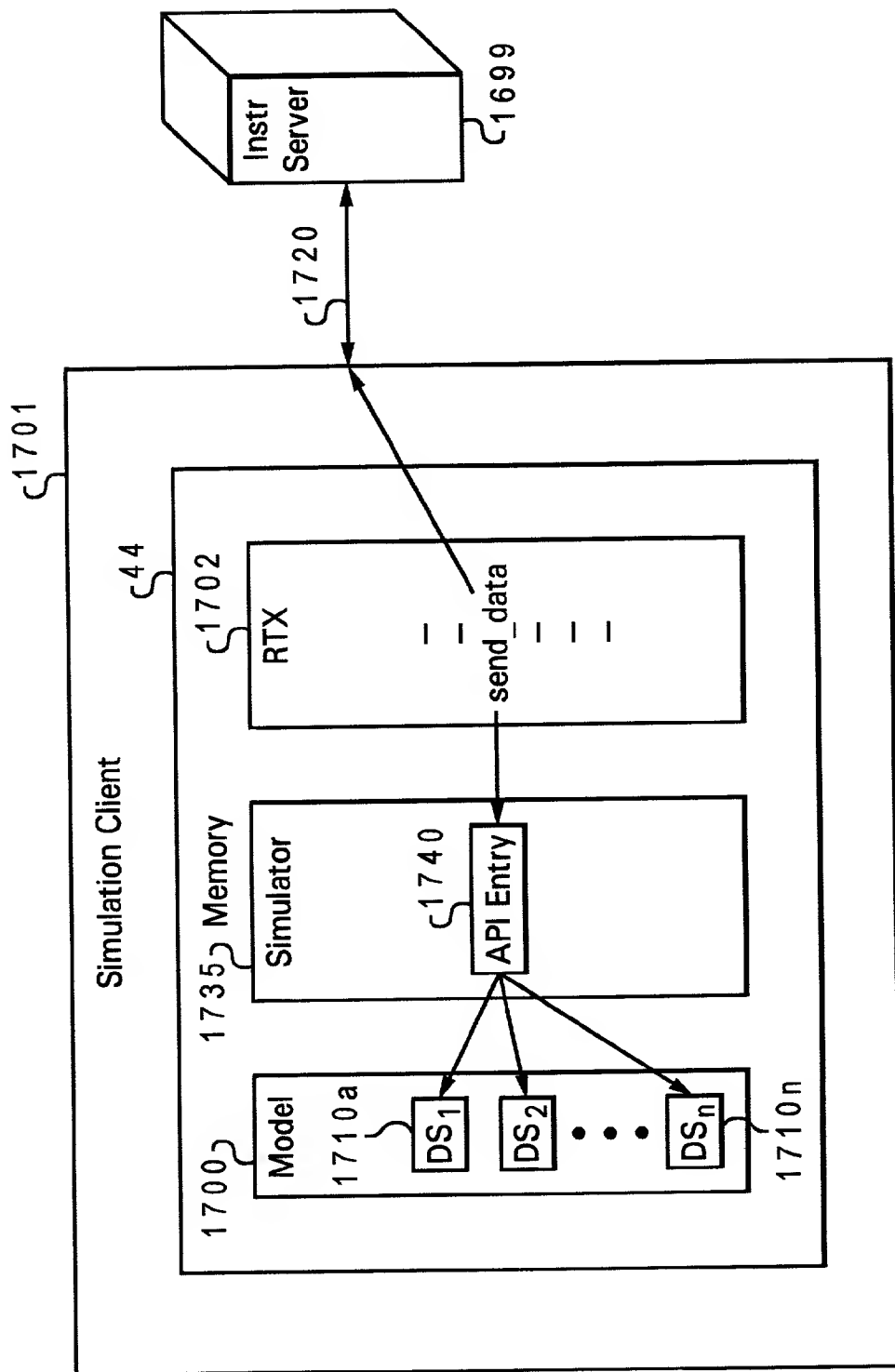


Fig. 17A

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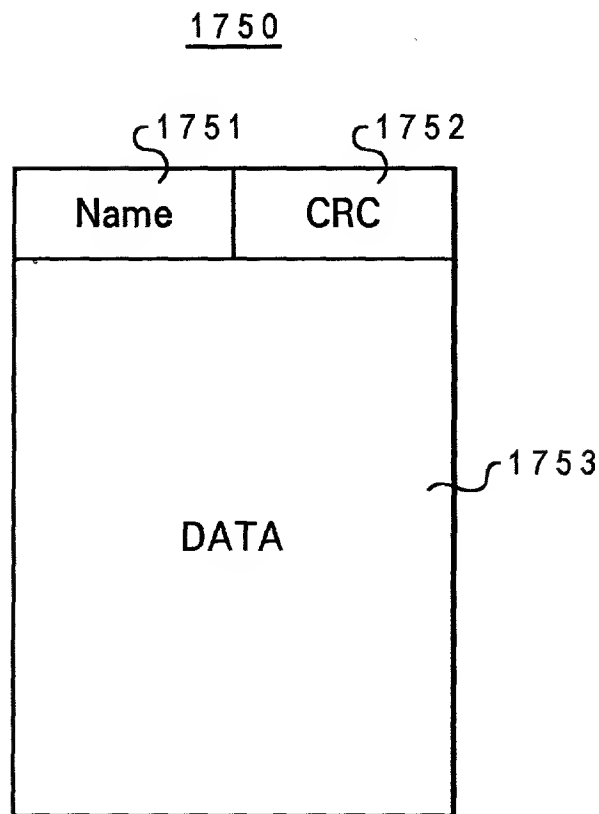


Fig. 17B

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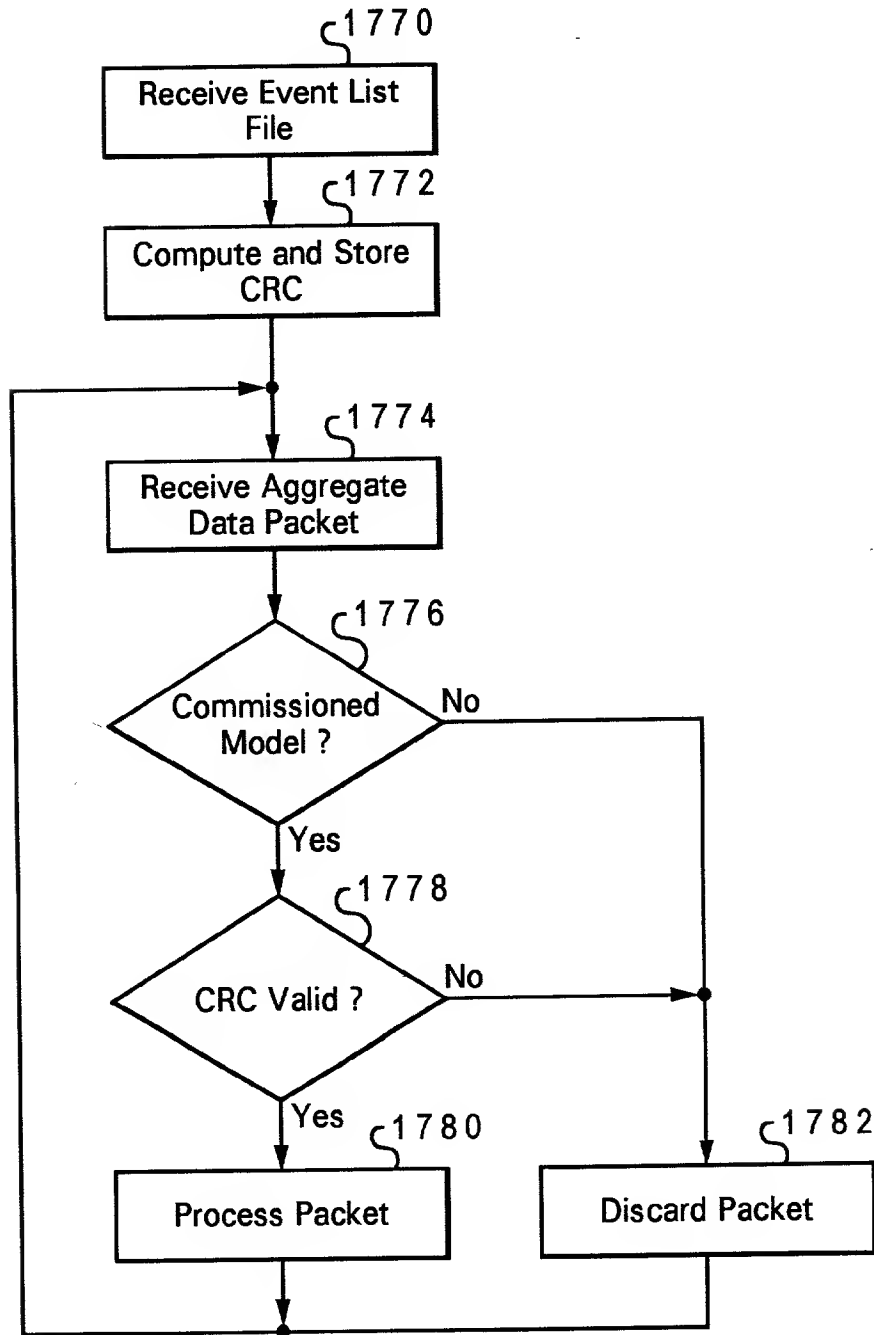


Fig. 17C

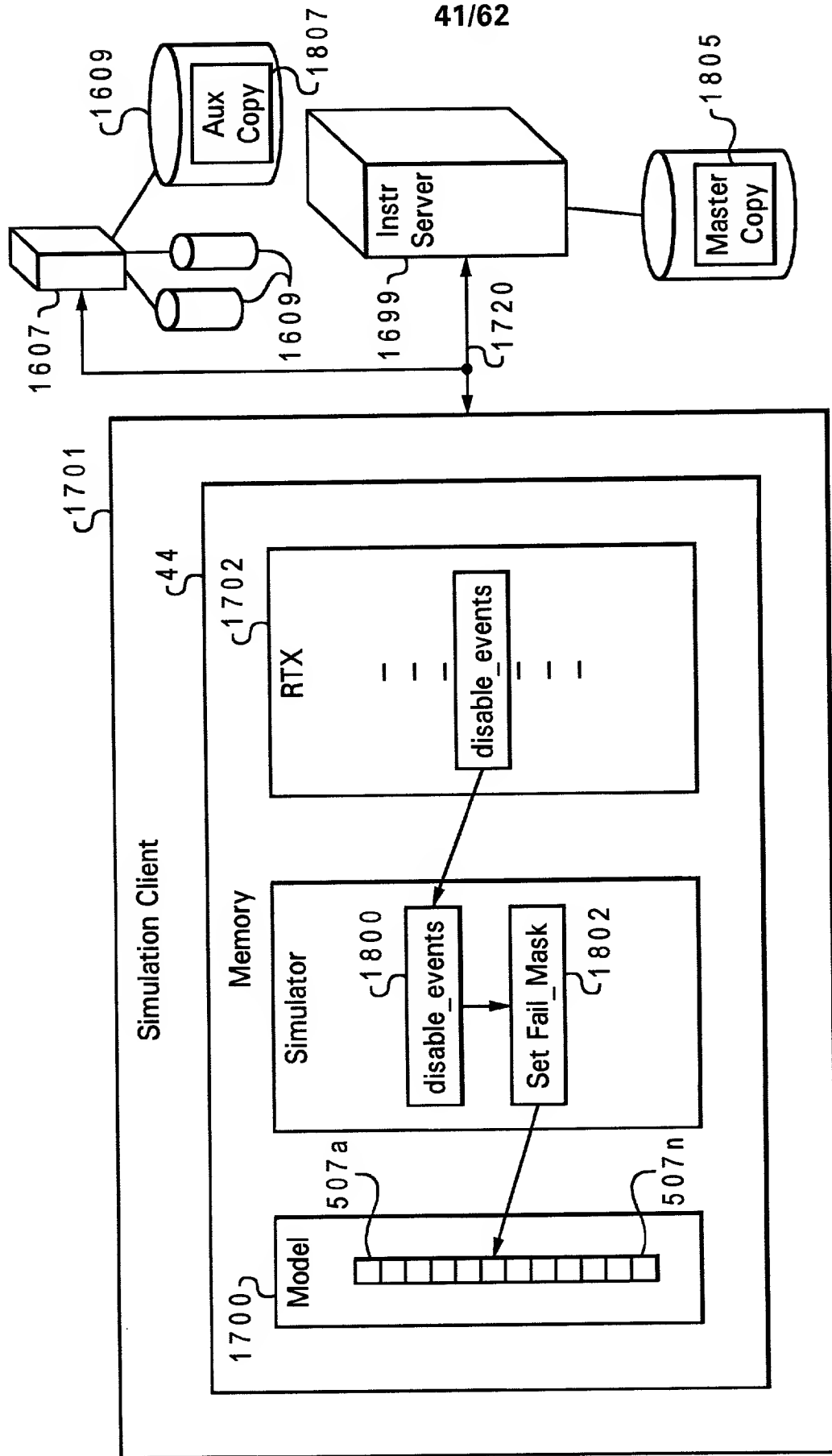
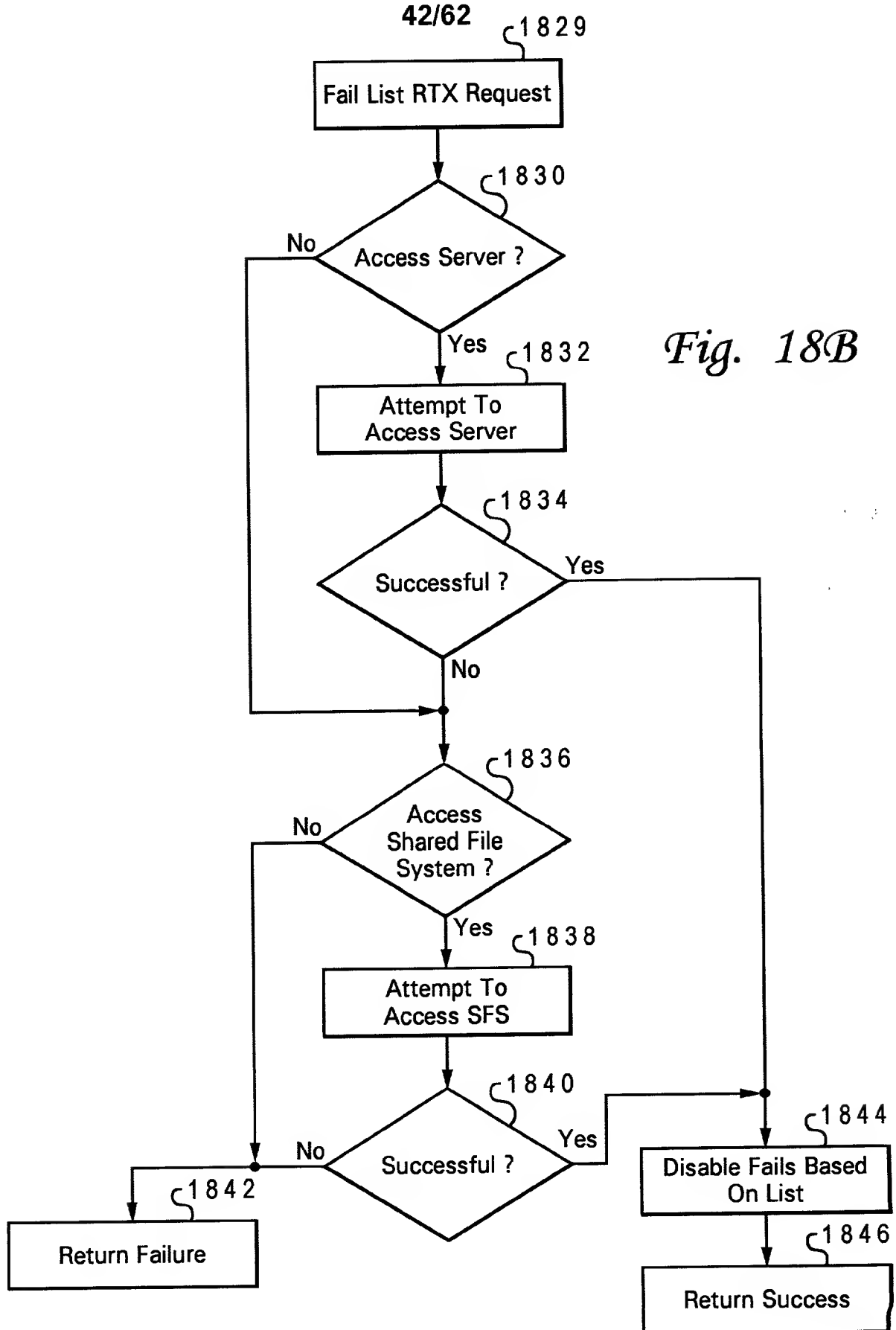


Fig. 18A

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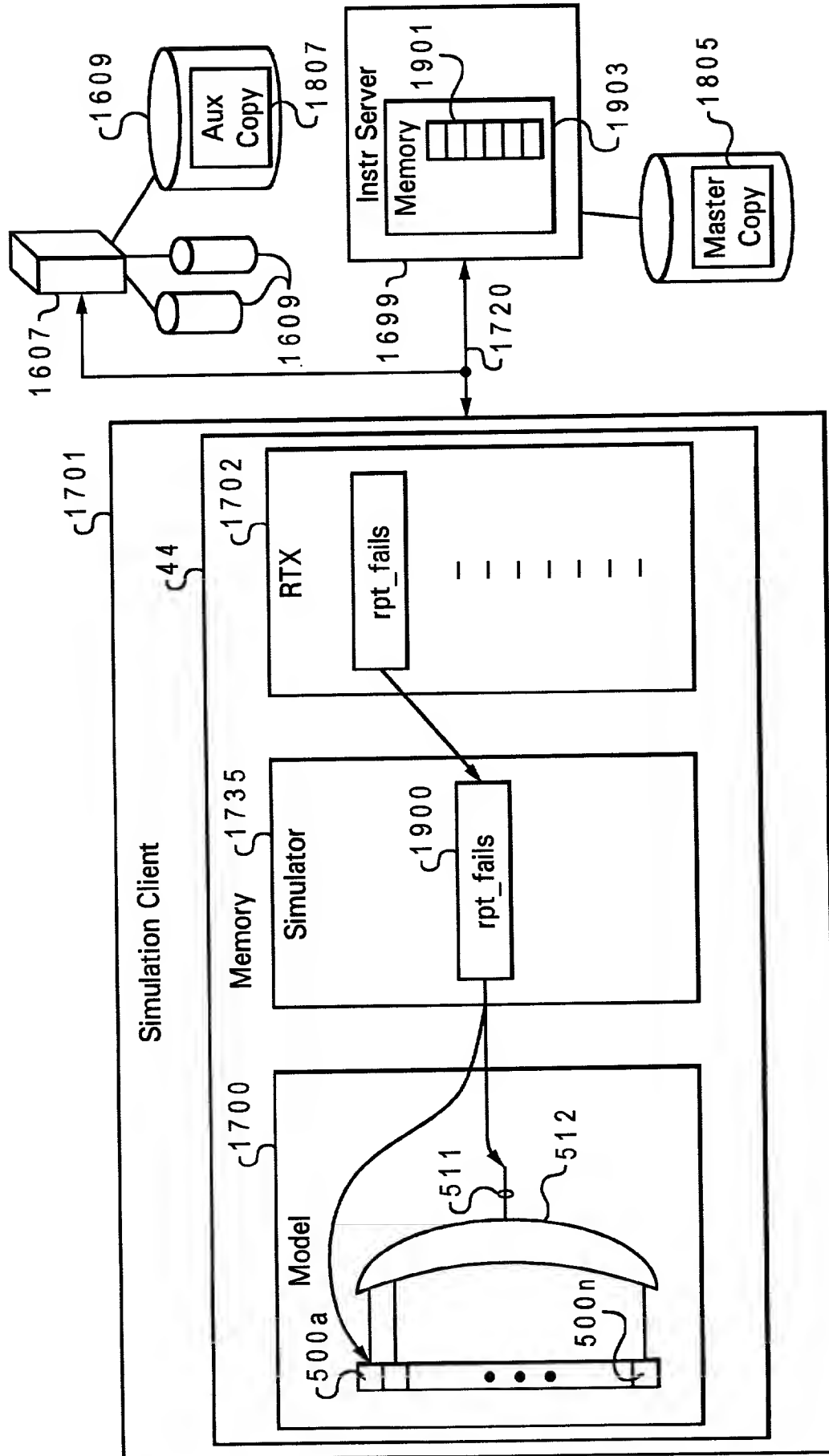
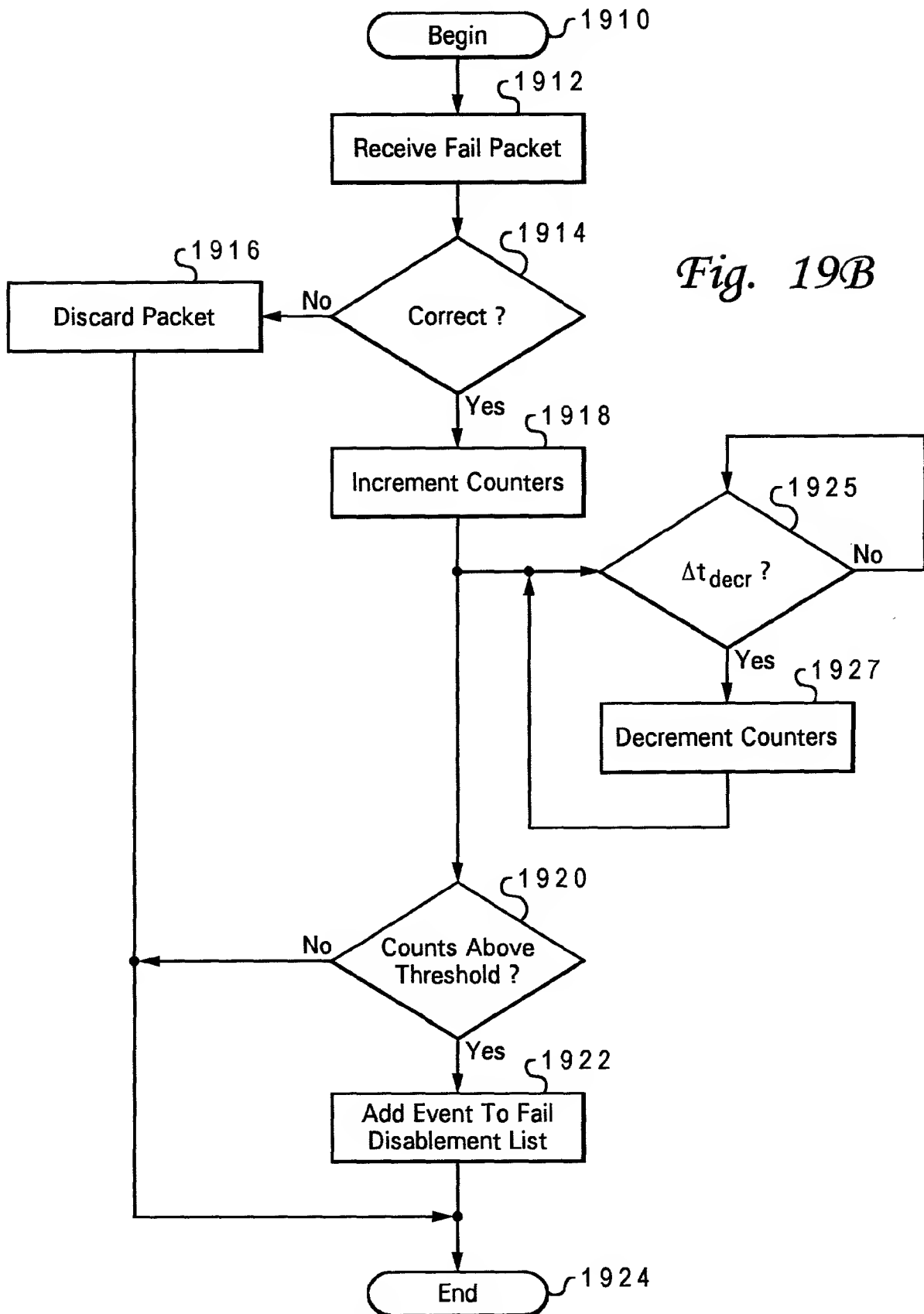


Fig. 19A

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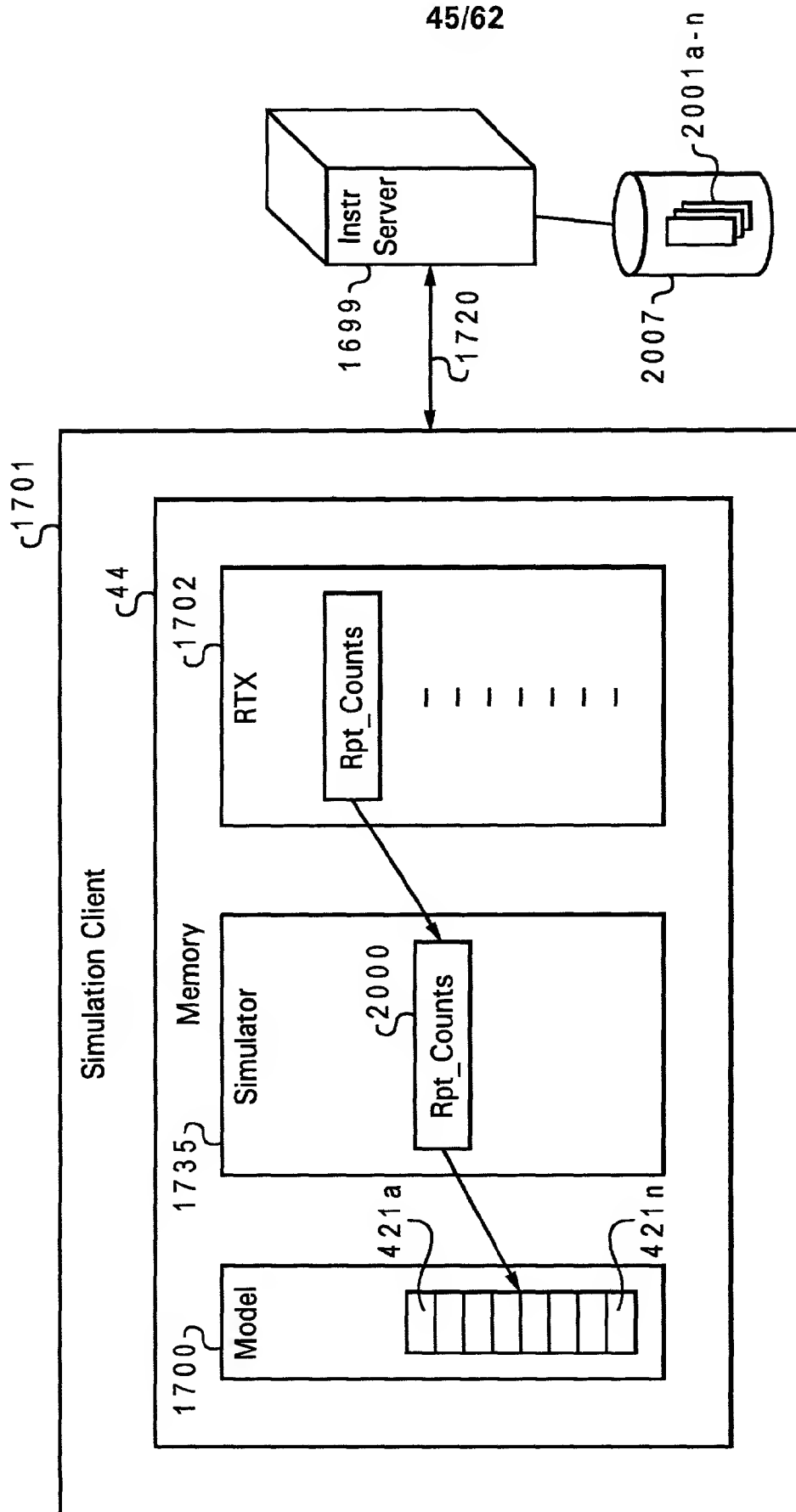


Fig. 20A

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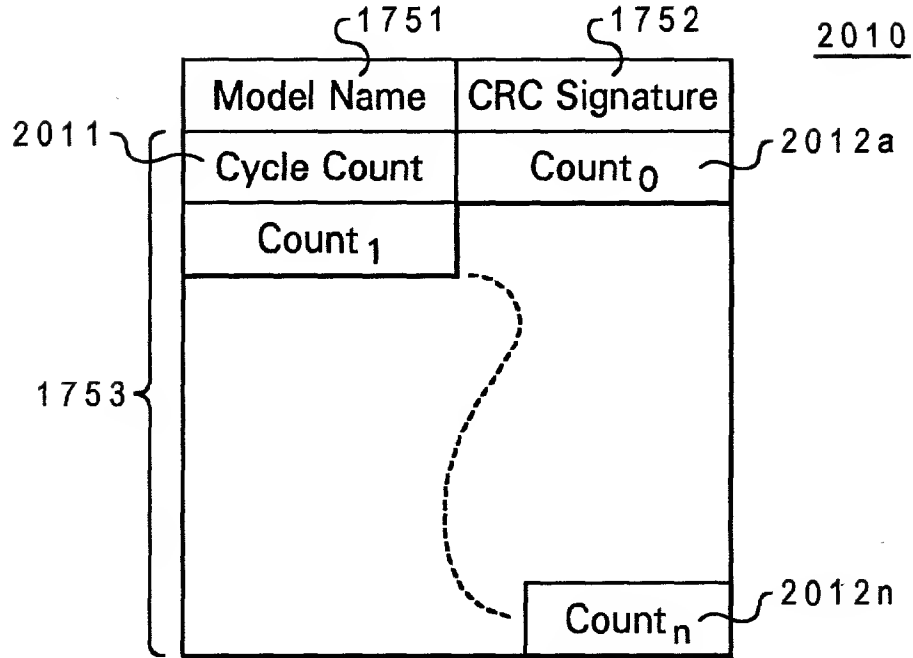


Fig. 20B

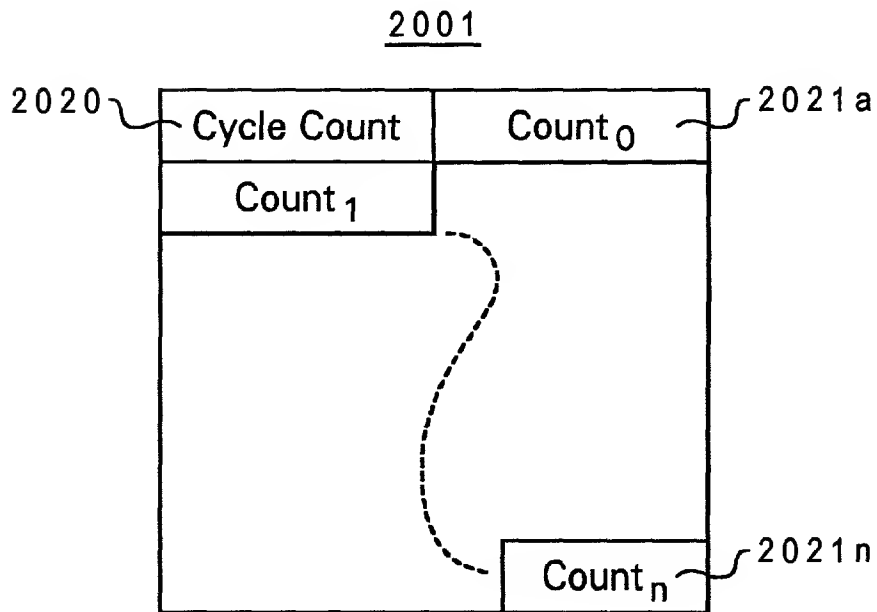


Fig. 20C

208000 0512.0000

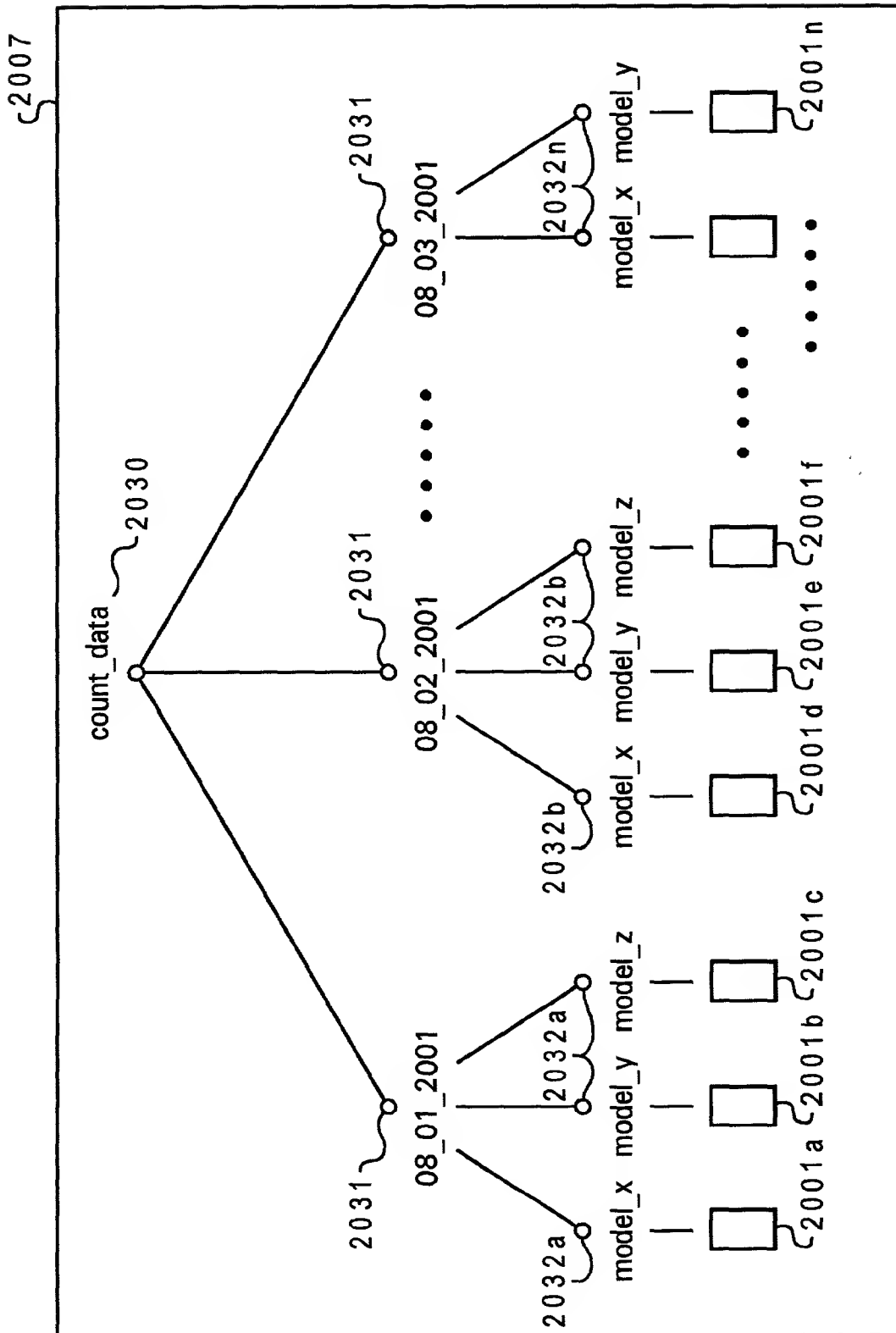


Fig. 20D

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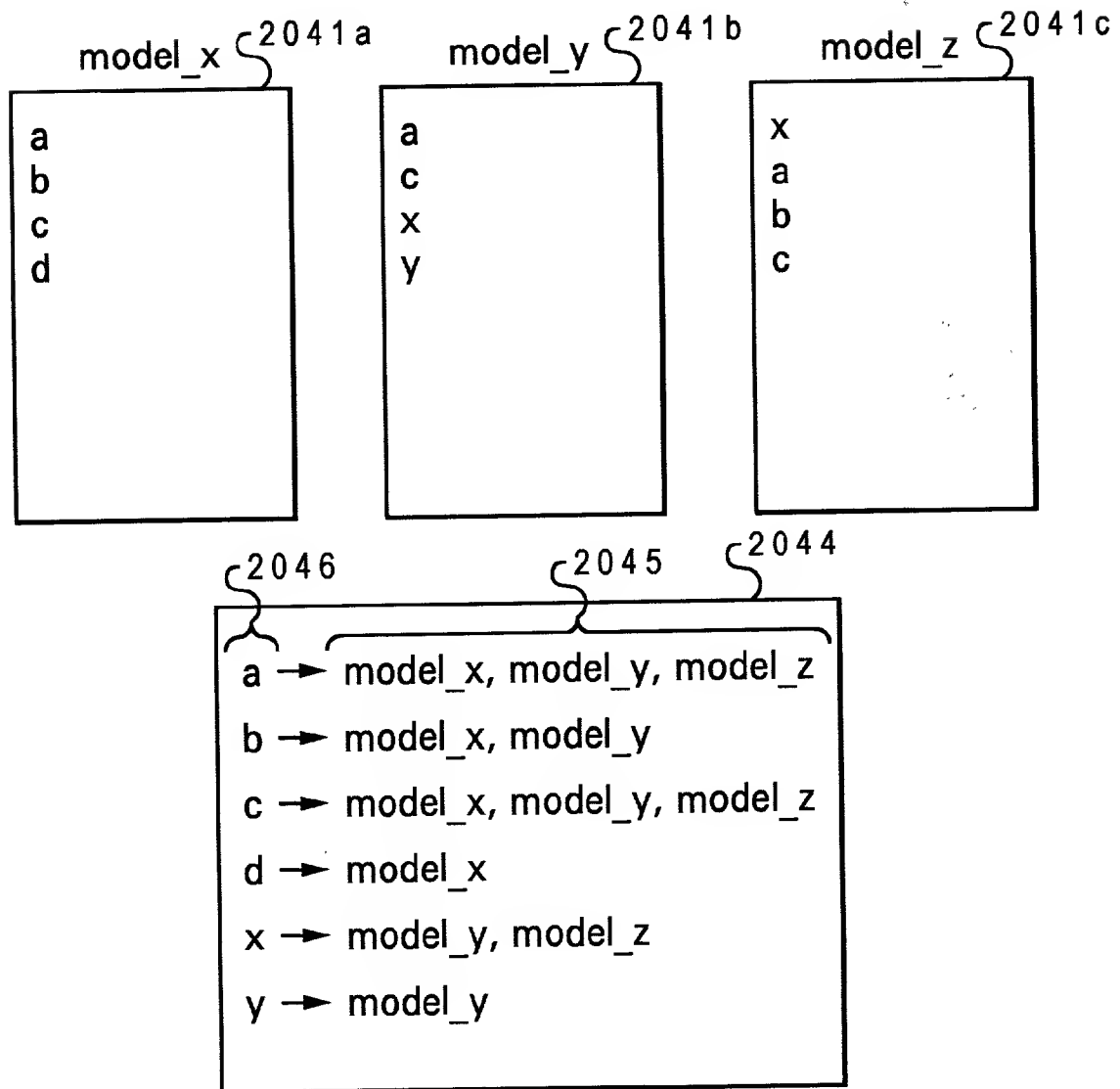
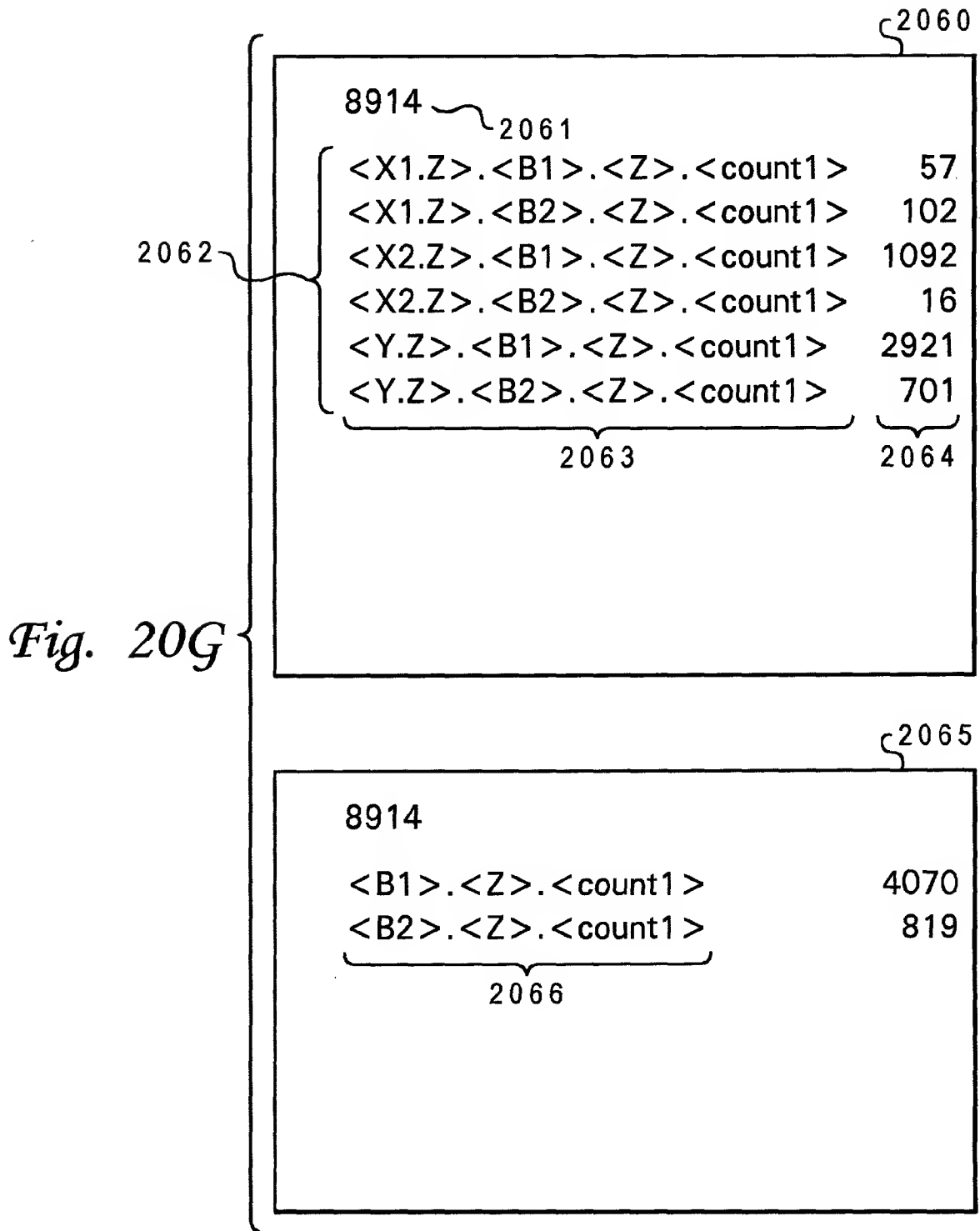


Fig. 20E

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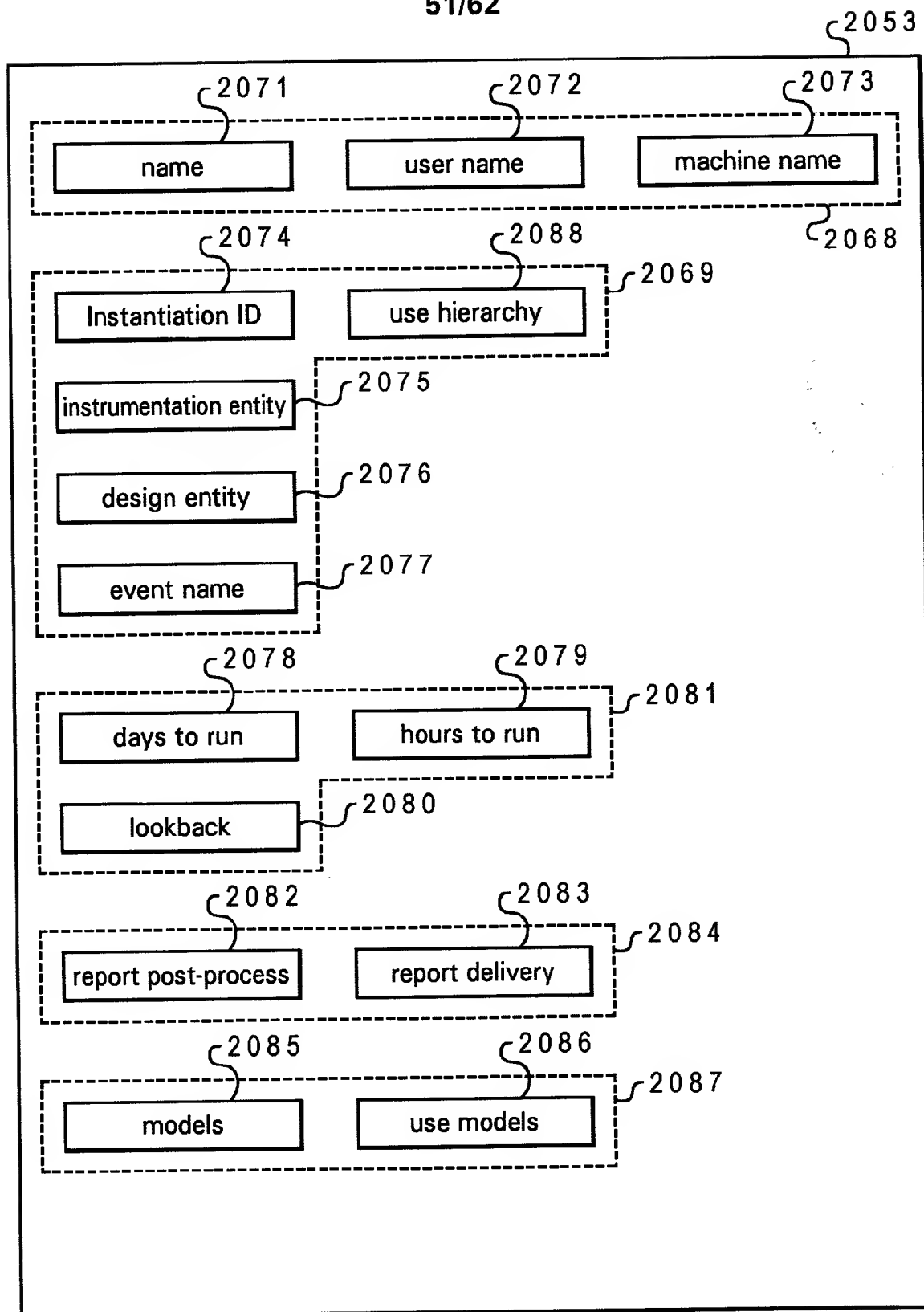


Fig. 20H

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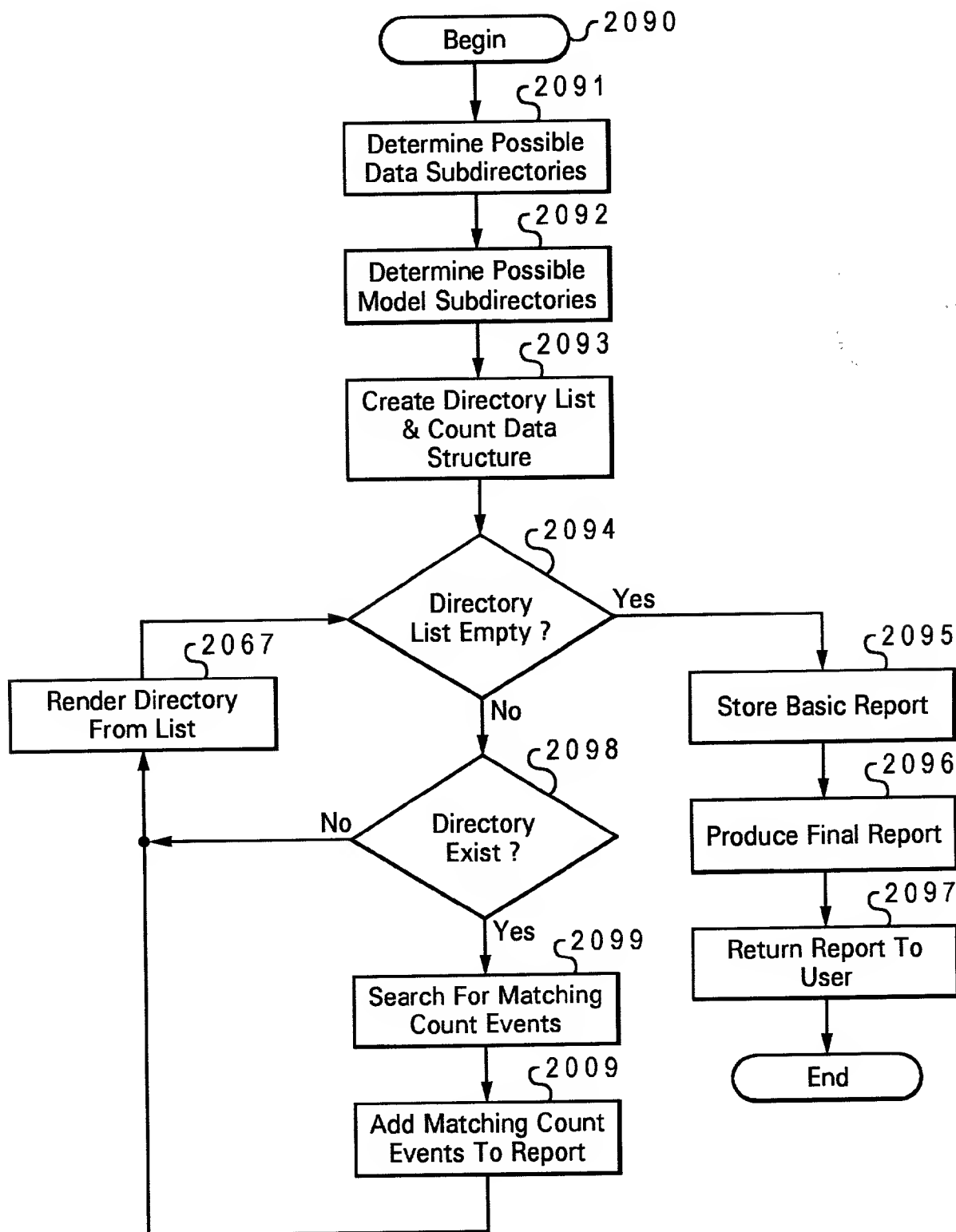


Fig. 20I

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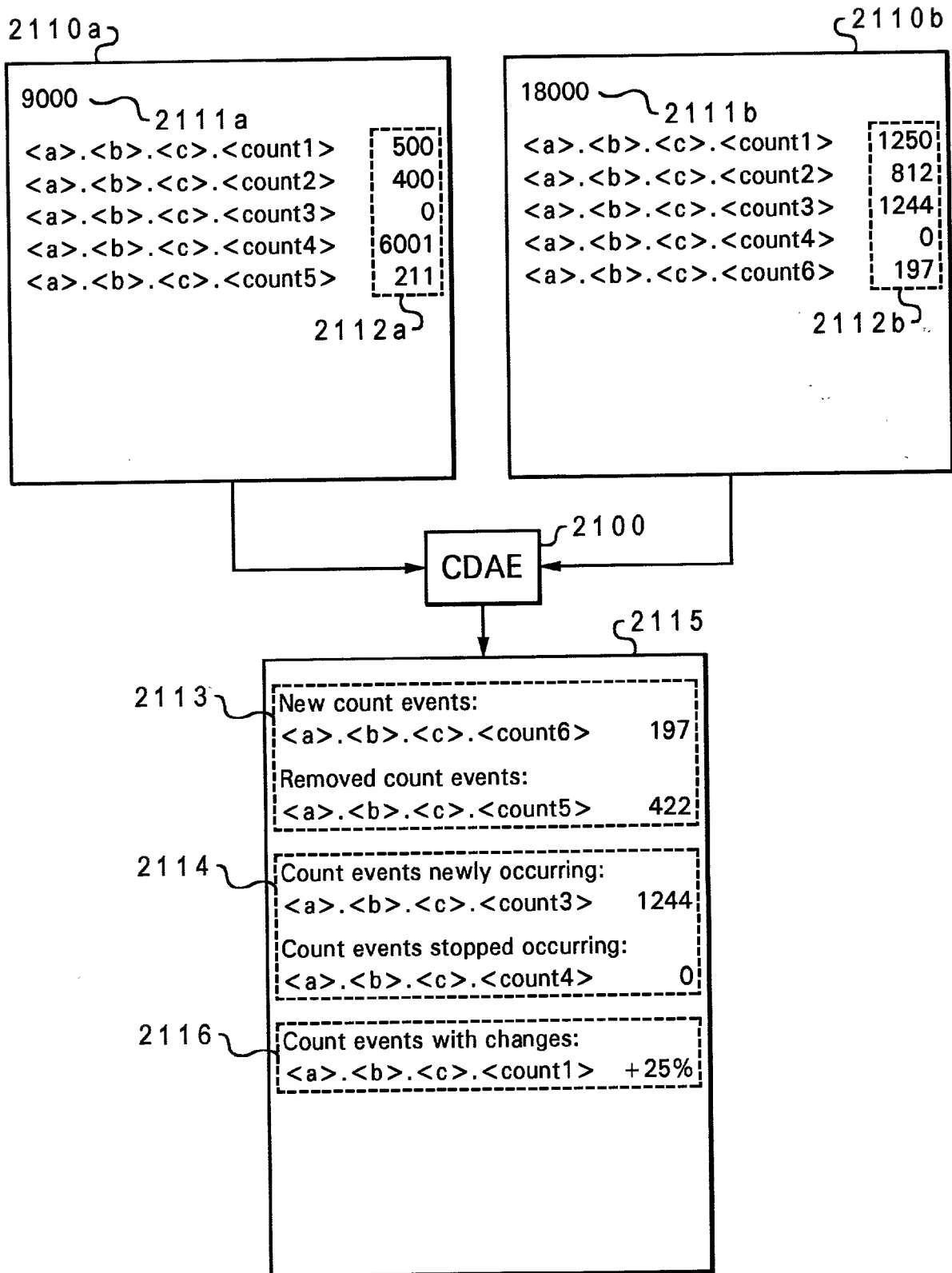


Fig. 21B

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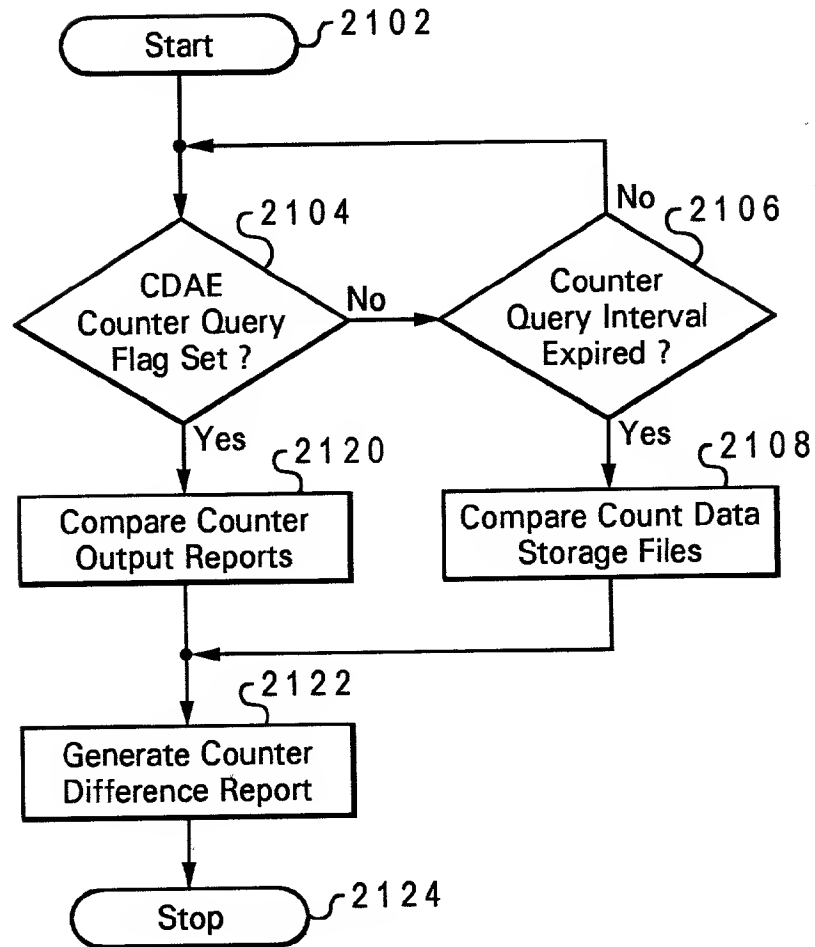
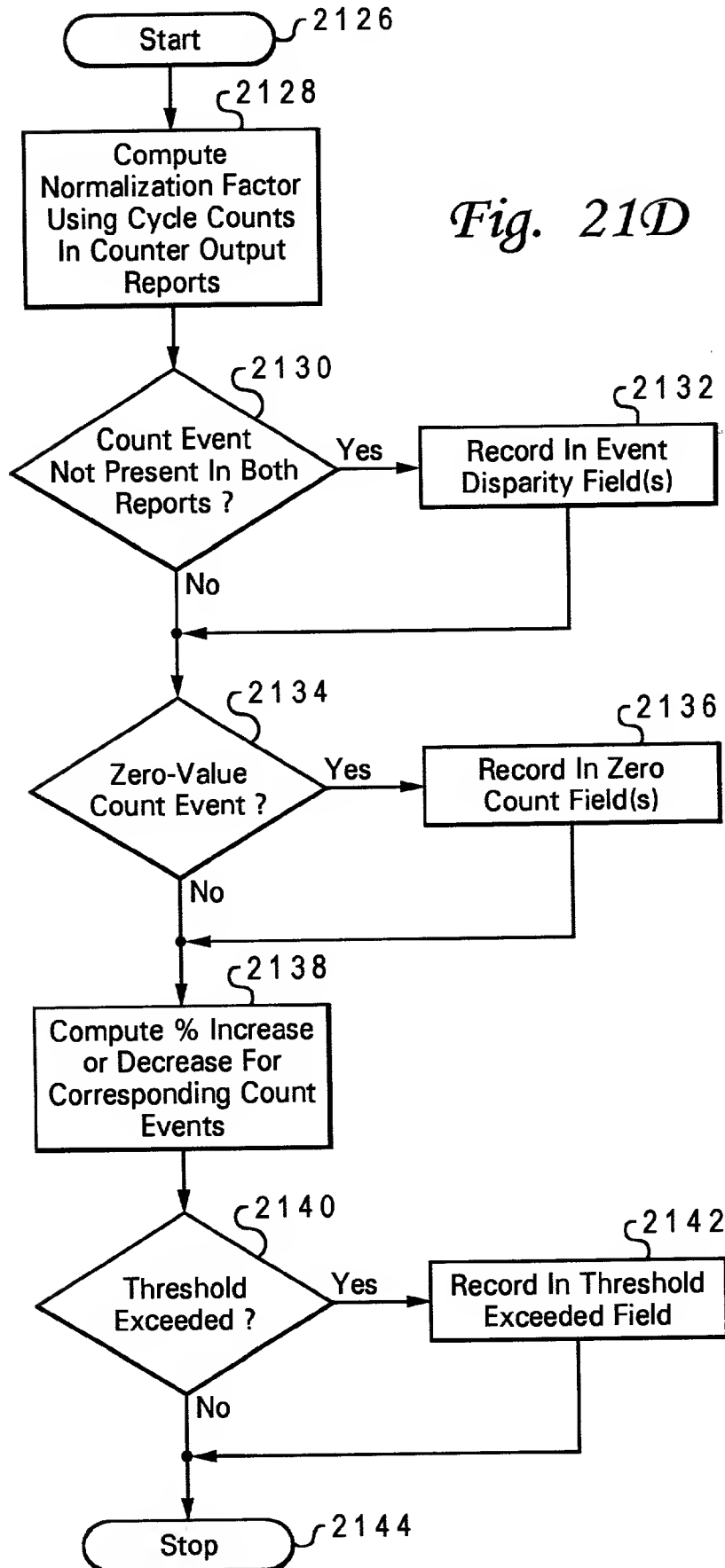


Fig. 21C



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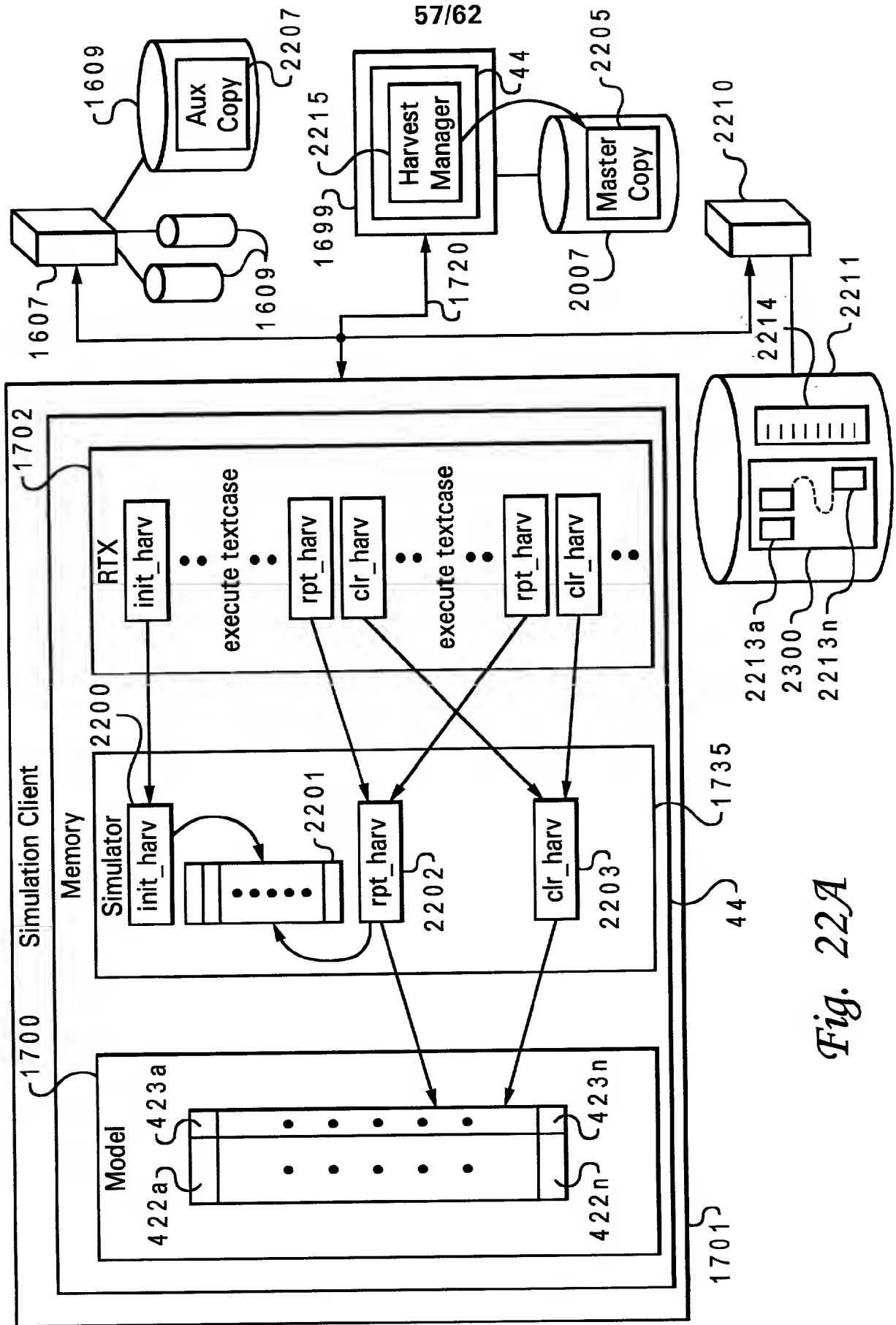
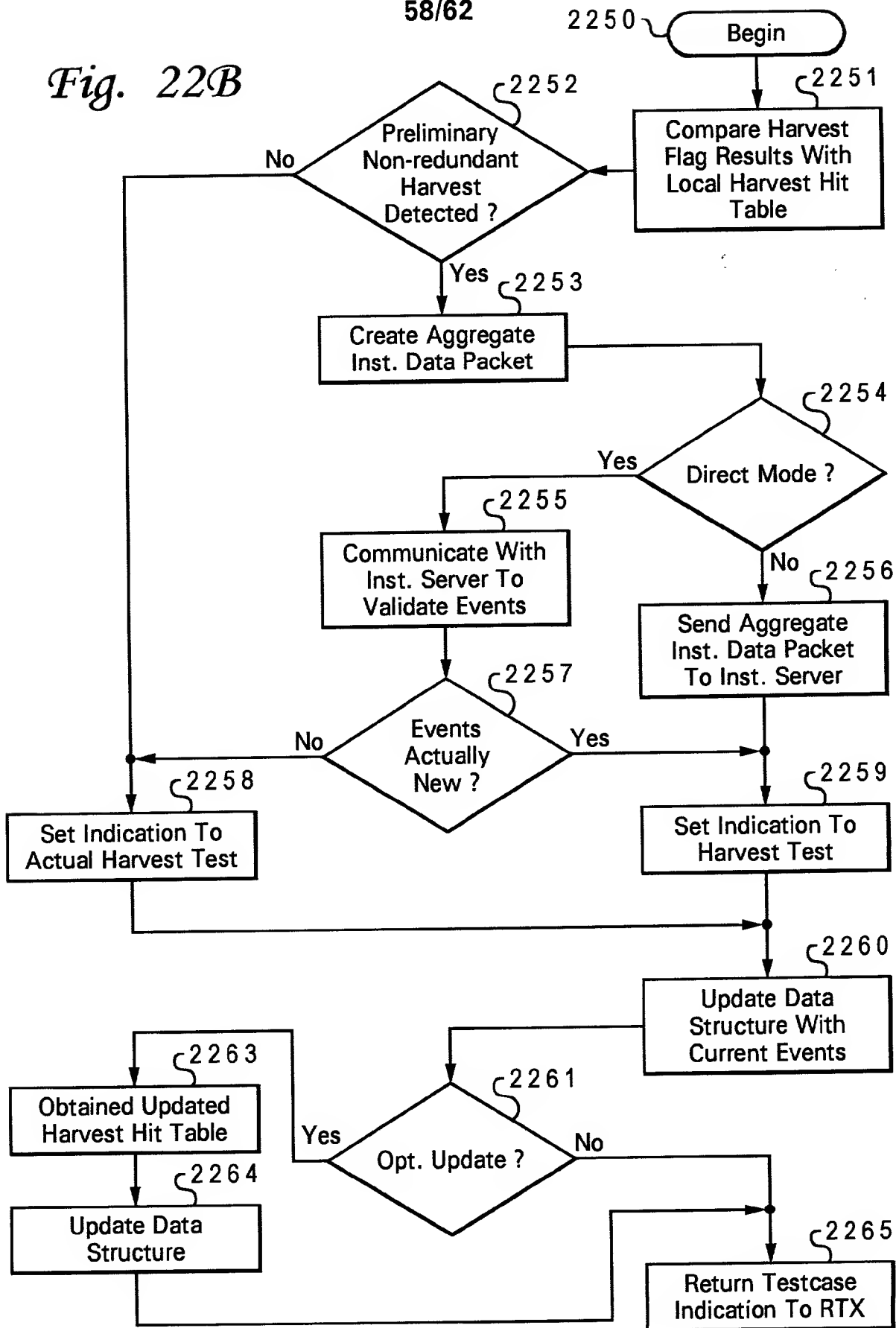


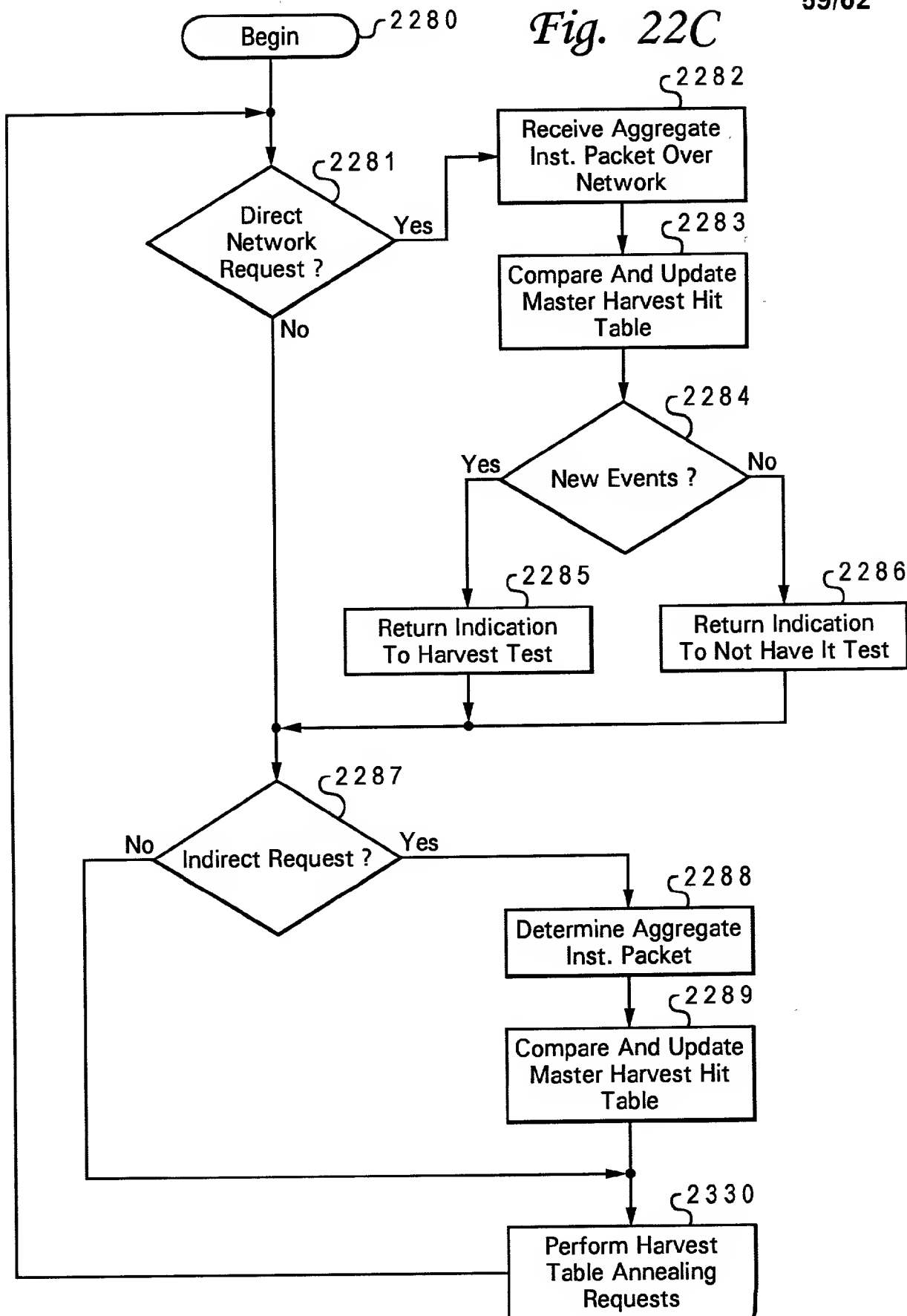
Fig. 22A

Fig. 22B



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Fig. 22C



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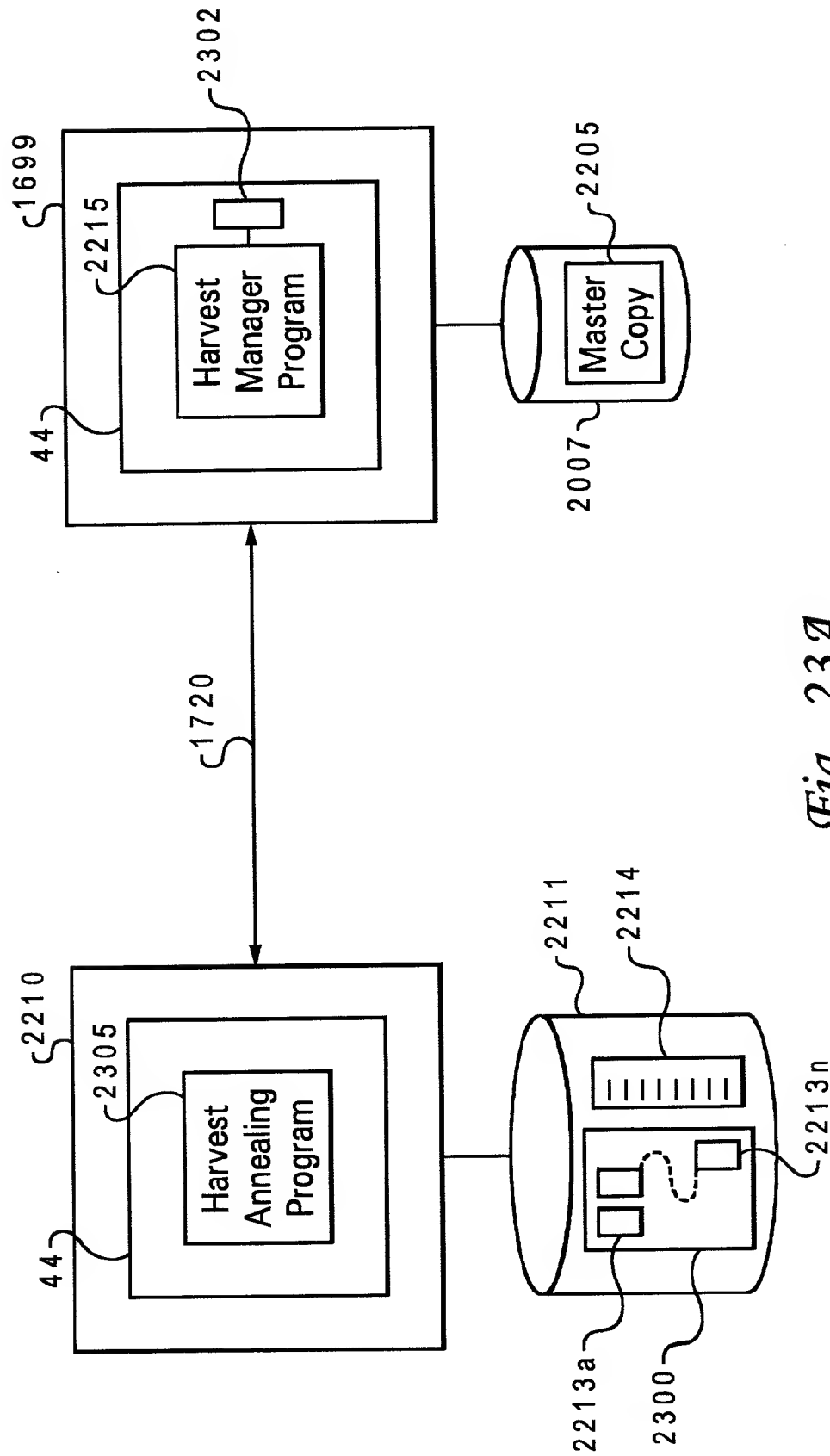


Fig. 23A

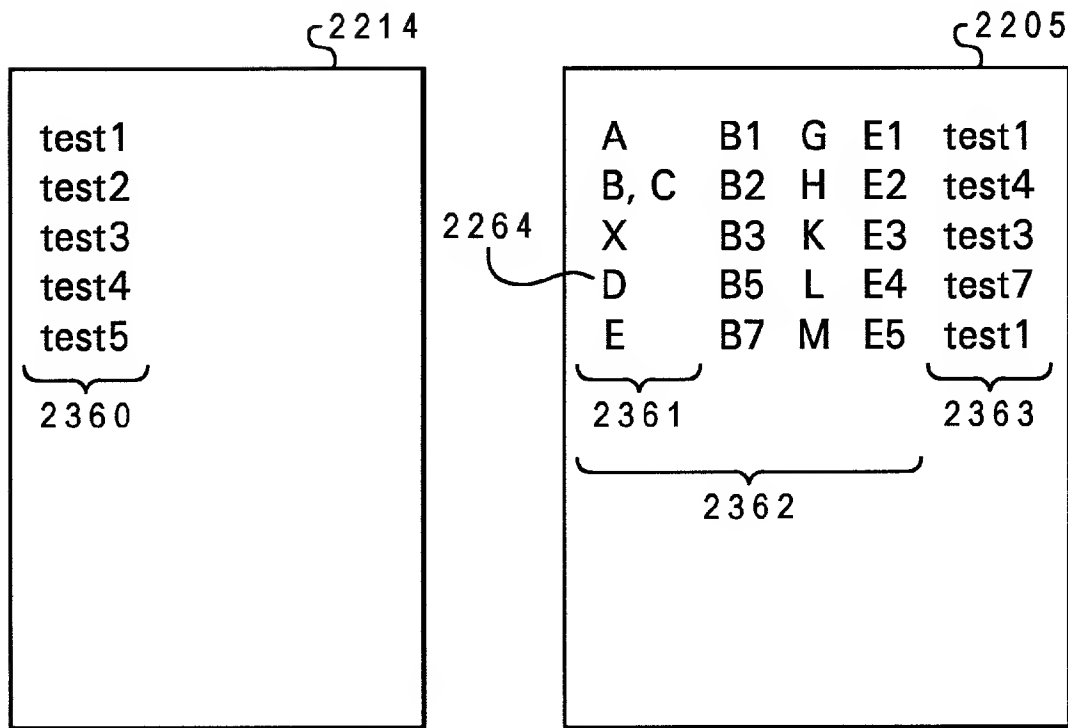


Fig. 23B

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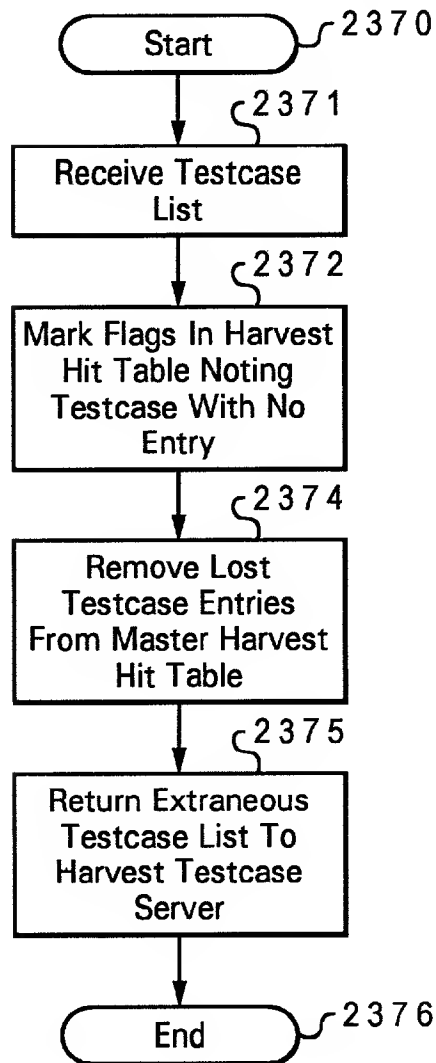


Fig. 23C